MP9472

0.45A, 18V, Non-Synchronous, Rectified, Step-Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP9472 is a monolithic, non-synchronous, buck regulator that integrates a 175mΩ high-side MOSFET to achieve 0.45A of continuous load current over a wide 4.75V to 18V input voltage range. Current mode control provides fast transient response and cycle-by-cycle current limit.

An adjustable soft-start prevents inrush current at start-up. The supply current drops to 1μA in shutdown mode.

The MP9472 requires minimal external components and is available in an 8-pin TSOT23-8 package.

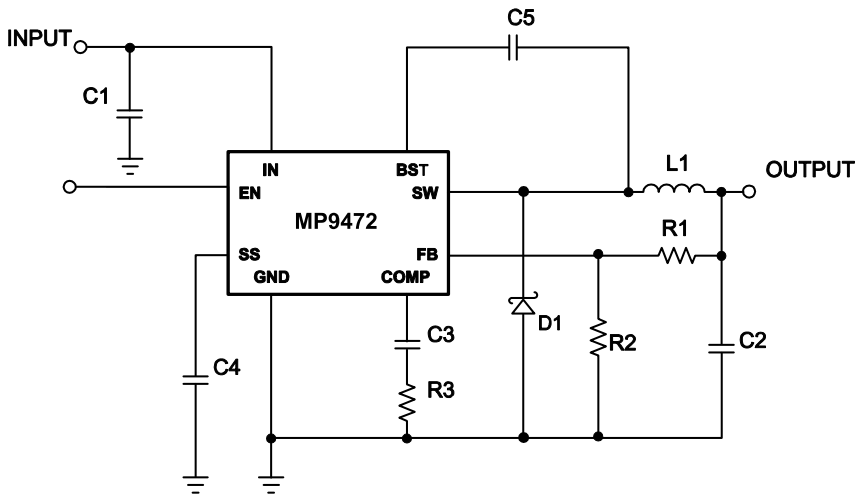
FEATURES

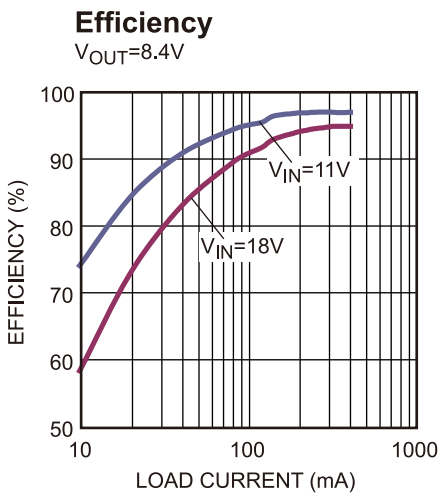
- 0.45A Output Current
- Wide 4.75V to 18V Operating Input Range
- Integrated High-Side Power MOSFET
- Output Adjustable from 0.923V to 15V
- Programmable Soft Start
- Stable with Low ESR Ceramic Output Capacitors
- Fixed 340kHz Frequency
- Cycle-by-Cycle Over-Current Protection (OCP)
- Input Under-Voltage Lockout (UVLO)
- 8-Pin TSOT23-8 Package

APPLICATIONS

- Distributed Power Systems
- Networking Systems
- FPGA, DSP, ASIC Power Supplies
- Green Electronics/Appliances
- Notebook Computers

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number	Package	Top Marking
MP9472GJ*	TSOT23-8	*See Below*

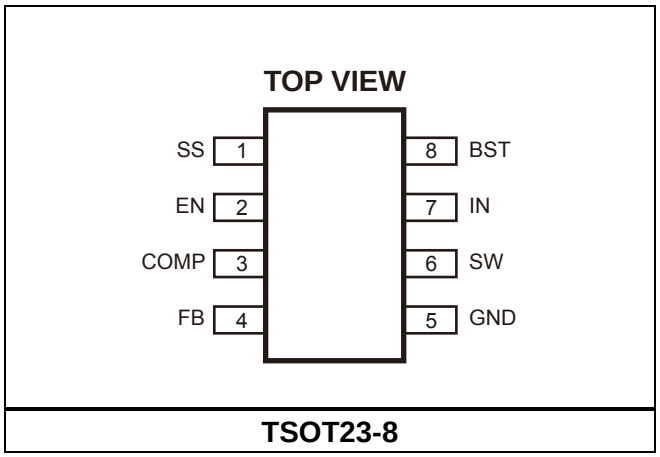
* For Tape & Reel, add suffix –Z (e.g. MP9472GJ–Z)

TOP MARKING

|APFY

APF: Product code of MP9472GJ
Y: Year code

PACKAGE REFERENCE



TSOT23-8

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) .....-0.3V to +20V
Switch node voltage (V_{SW}) 21V
Boost voltage (V_{BST})..... V_{SW} - 0.3V to V_{SW} + 6V
All other pins .....-0.3V to +6V
Junction temperature .....150°C
Continuous power dissipation (T_A = +25°C) (2)
……1.25W
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Input voltage (V_{IN}) .....4.75V to 18V
Output voltage (V_{OUT}).....0.923V to 15V
Maximum junction temp. (T_J) .....+125°C

Thermal Resistance (4)	θ_{JA}	θ_{JC}	
TSOT23-8	100	55	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to 125°C. Typical value is tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Shutdown supply current		V_{EN} = 0V, T_J = 25°C			1	μA
Supply current		V_{EN} = 5.0V, V_{FB} = 1.0V		1.3	1.8	mA
Feedback voltage	V_{FB}	4.75V ≤ V_{IN} ≤ 18V	0.900	0.923	0.946	V
		V_{IN} = 12V	0.905	0.923	0.941	V
Feedback reference voltage drift(5)		20°C ≤ T_J ≤ 50°C	-2		2	mV
Feedback overvoltage threshold				1.1		V
Error amplifier voltage gain(6)	A_{EA}			400		V/V
Error amplifier transconductance	G_{EA}	ΔI_C = ±10μA		800		μA/V
High-side switch on resistance(6)	$R_{DS(ON)}$			175		mΩ
High-side switch leakage current		V_{EN} = 0V, V_{SW} = 0V			10	μA
Upper switch current limit		Duty = 80%, T_J = 25°C	0.5	1		A
COMP to current sense transconductance	GCS			3.5		A/V
Oscillation frequency	F_{osc1}		300	340	380	kHz
Short-circuit oscillation frequency	F_{osc2}	V_{FB} = 0V		100		kHz
Maximum duty cycle(5)	D_{MAX}	V_{FB} = 0.8V, 20°C ≤ T_J ≤ 50°C	86	90		%
Minimum on time (5)				220		ns
EN shutdown threshold voltage		V_{EN} rising	1.1	1.5	2.0	V
EN shutdown threshold voltage hysteresis				210		mV
EN lockout threshold voltage			2.2	2.5	2.7	V
EN lockout hysteresis				210		mV
Input under-voltage lockout threshold		V_{IN} rising		3.80	4.50	V
Input under-voltage lockout threshold hysteresis				210		mV
Soft-start current		V_{SS} = 0V		6		μA
Soft-start period		C_{SS} = 0.1μF		15		ms
Thermal shutdown entry(5)				160		°C
Thermal shutdown threshold hysteresis (5)				30		°C

NOTES:

5) Guaranteed by characterization, not production tested.

6) Guaranteed by design

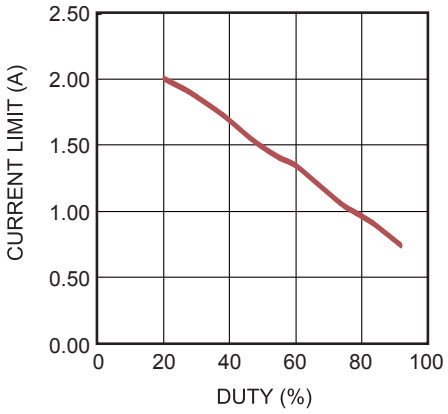
PIN FUNCTIONS

Pin #	Name	Description
1	SS	**Soft-start control input.** SS controls the soft-start period. Connect a capacitor from SS to GND to set the soft-start period. A 0.1µF capacitor sets the soft-start period to 15ms. To disable the soft-start feature, leave SS unconnected.
2	EN	**Enable input.** EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. Pull EN up with a 100kΩ resistor for automatic start-up.
3	COMP	**Compensation node.** Connect a series RC network from COMP to GND to compensate for the regulation control loop. In some cases, an additional capacitor from COMP to GND is required. See the Compensation Components section on page 12 for details.
4	FB	**Feedback input.** FB senses and regulates the output voltage. Drive FB with a resistive voltage divider from the output voltage. The feedback threshold is 0.923V. See the Setting the Output Voltage section on page 11 for details.
5	GND	**Ground.**
6	SW	**Power switching output.** SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load and a low V_F Schottky rectifier to ground. Note that a capacitor is required from SW to BST to power the high-side switch.
7	IN	**Power input.** IN supplies power to the IC, as well as the step-down converter switches. Drive IN with a 4.75V to 18V power source. Bypass IN to GND with a sufficiently large capacitor to eliminate noise on the input to the IC. See the Selecting the Input Capacitor section on page 11 for details.
8	BST	**High-side gate drive boost input.** BST supplies the drive for the high-side N-channel MOSFET switch. Connect a 0.01µF capacitor from SW to BST to power the high-side switch.

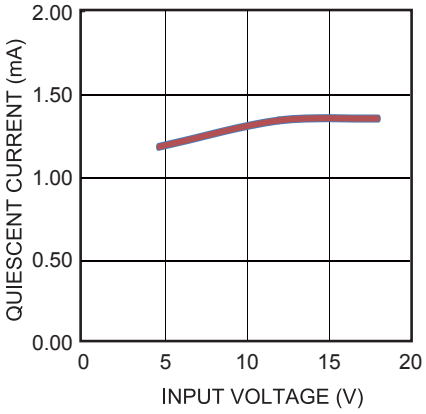
TYPICAL PERFORMANCE CHRACTERISTICS

V_{IN} = 11V, V_{OUT} = 8.4V, L = 120µH, unless otherwise noted.

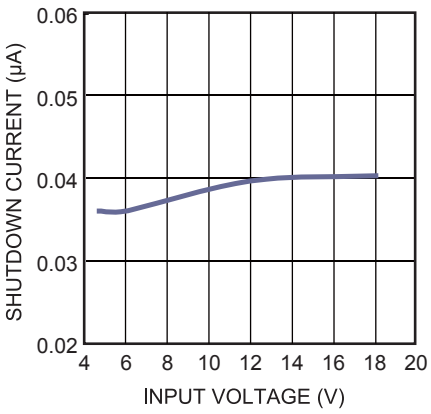
Current Limit vs. Duty Cycle



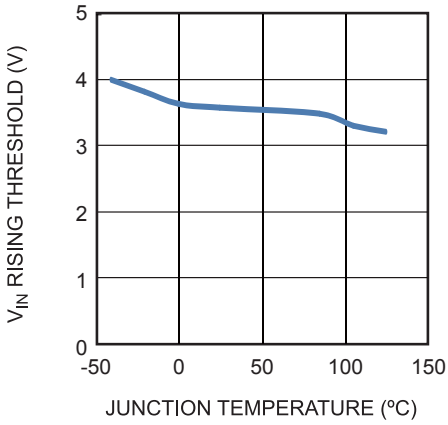
Quiescent Current vs. Input Voltage



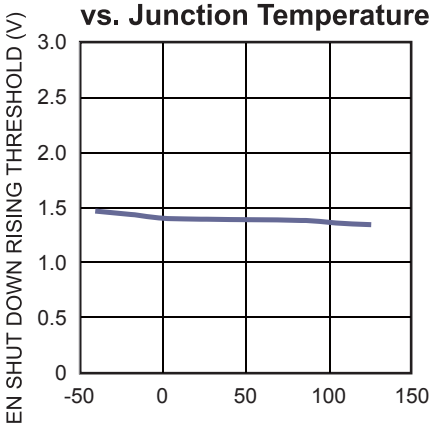
Shutdown Current vs. Input Voltage



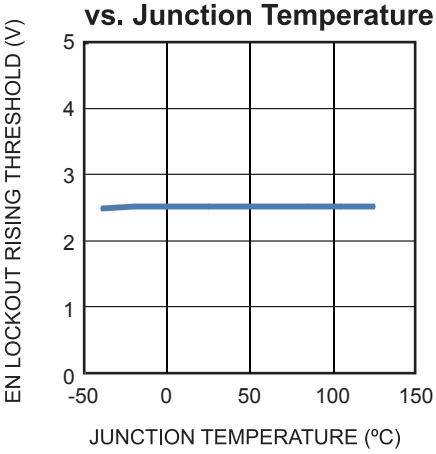
V_{IN} Rising Threshold vs. Junction Temperature



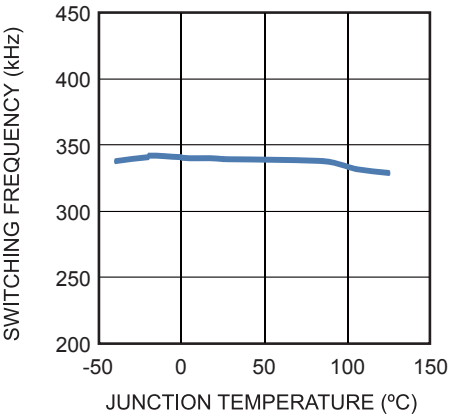
EN Shutdown Rising Threshold vs. Junction Temperature



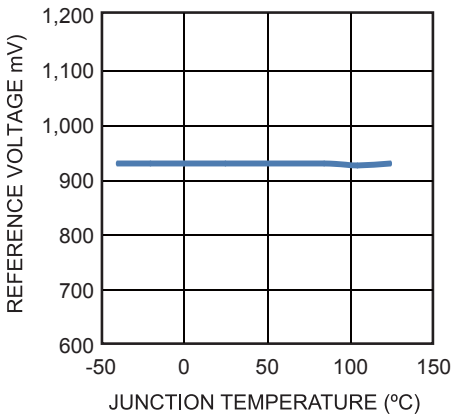
EN Lockout Rising Threshold vs. Junction Temperature



Switching Frequency vs. Junction Temperature



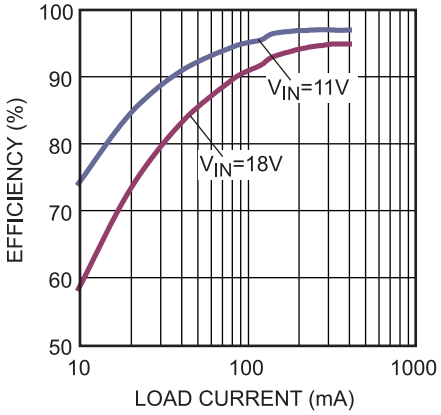
Reference Voltage vs. Junction Temperature



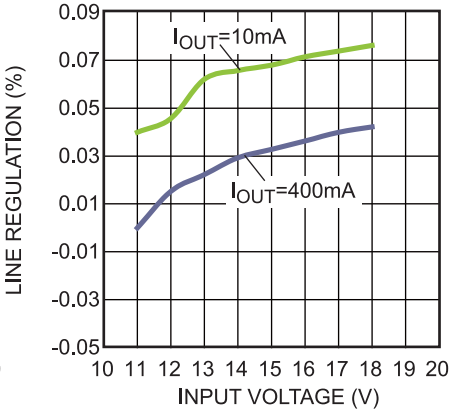
TYPICAL PERFORMANCE CHRACTERISTICS *(continued)*

V_{IN} = 11V, V_{OUT} = 8.4V, L = 120µH, unless otherwise noted.

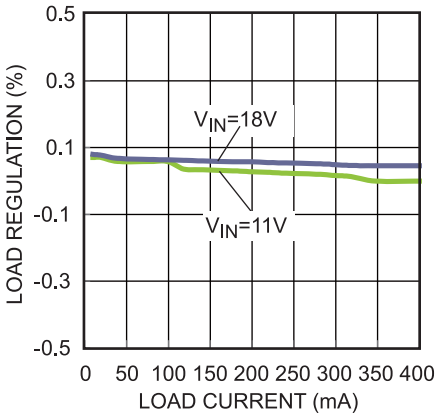
Efficiency



Line Regulation

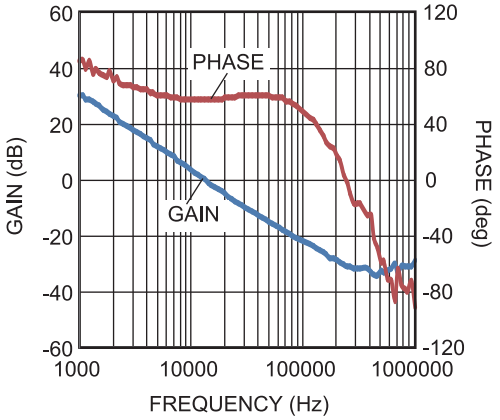


Load Regulation



Bode Plot

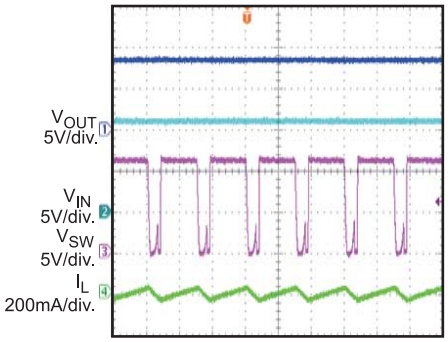
I_{OUT}=0.4A



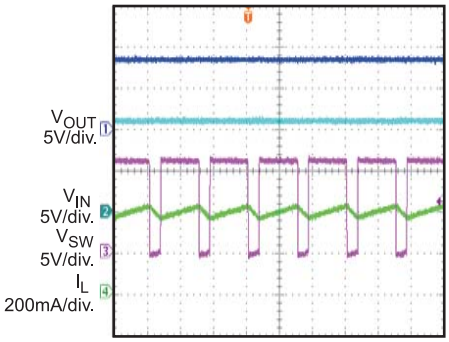
TYPICAL PERFORMANCE CHRACTERISTICS *(continued)*

V_{IN} = 11V, V_{OUT} = 8.4V, L = 120µH, unless otherwise noted.

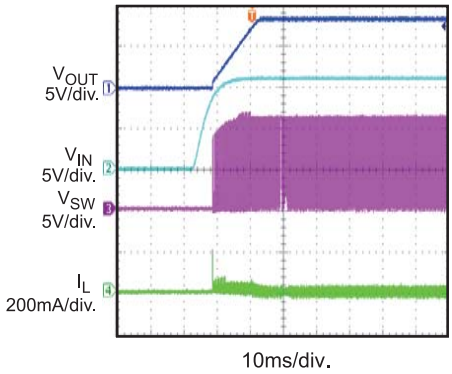
Steady State
I_{OUT} = 0A



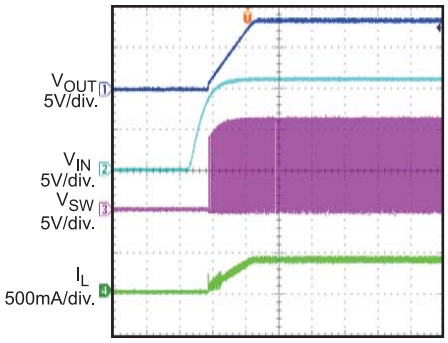
Steady State
I_{OUT} = 0.4A



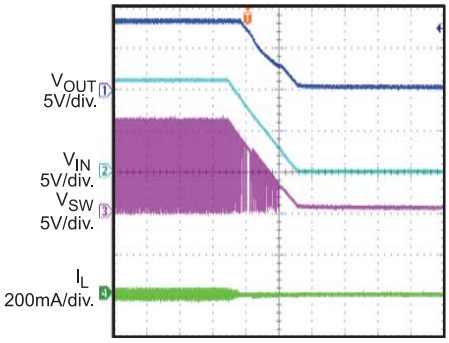
V_{IN} Start-Up
I_{OUT} = 0A



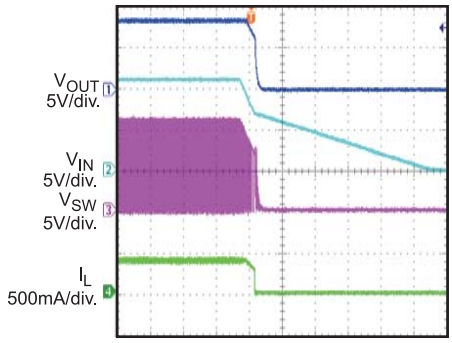
V_{IN} Start-Up
I_{OUT} = 0.4A



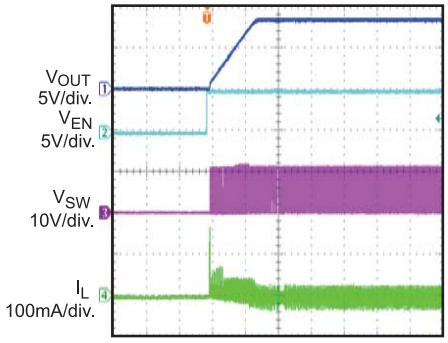
V_{IN} Shutdown
I_{OUT} = 0A



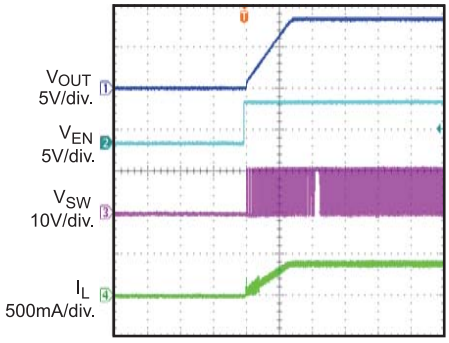
V_{IN} Shutdown
I_{OUT} = 0.4A



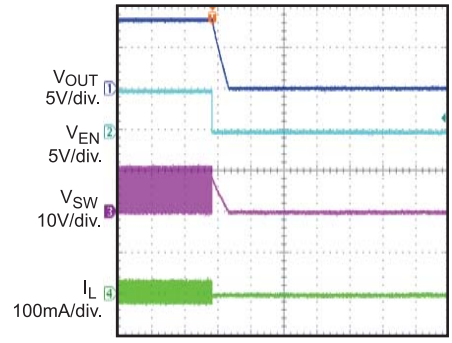
EN Start-Up
I_{OUT} = 0A



EN Start-Up
I_{OUT} = 0.4A



EN Shutdown
I_{OUT} = 0A

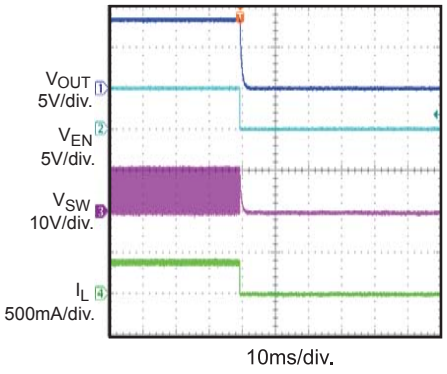


TYPICAL PERFORMANCE CHRACTERISTICS *(continued)*

V_{IN} = 11V, V_{OUT} = 8.4V, L = 120µH, unless otherwise noted.

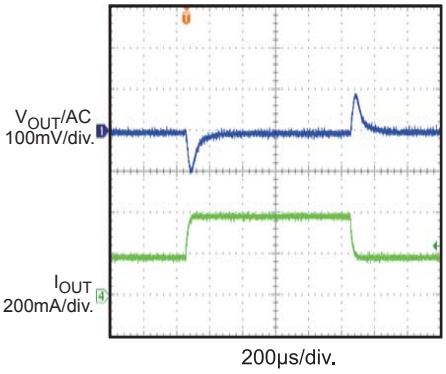
EN Shutdown

I_{OUT} = 0.4A



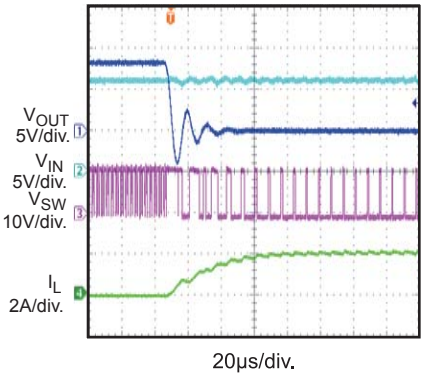
Load Transient

I_{OUT} = 0.2A to 0.4A



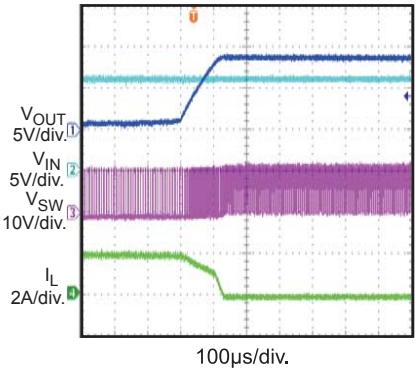
Short Entry

I_{OUT} = 0A



Short Recovery

I_{OUT} = 0A



OPERATION

The MP9472 is a non-synchronous, current-mode, step-down regulator. It regulates input voltages from 4.75V to 18V down to output voltages as low as 0.923V and supplies up to 0.45A of load current.

The MP9472 uses current-mode control to regulate the output voltage. The output voltage is measured at FB through a resistive voltage divider and amplified through the internal trans-conductance error amplifier.

The voltage at COMP is compared to the switch current and is measured internally to control the output voltage. The MP9472 stops switching once the COMP voltage drops to about 920mV in light-load condition.

The converter uses an internal N-channel MOSFET switch to step down the input voltage to the regulated output voltage. Since the high-side MOSFET requires a gate voltage greater than the input voltage, a boost capacitor connected between SW and BST is needed to drive the high-side gate. The boost capacitor is charged from the internal 5V rail when SW is low. To maintain normal regulation, a certain amount of loading current is always required to pull SW to 0V at every cycle so the boost capacitor can be charged by an internal 5V rail.

When FB exceeds 20% of the nominal regulation voltage (0.923V), the over-voltage comparator is tripped, and COMP and SS are discharged to GND, forcing the high-side switch off.

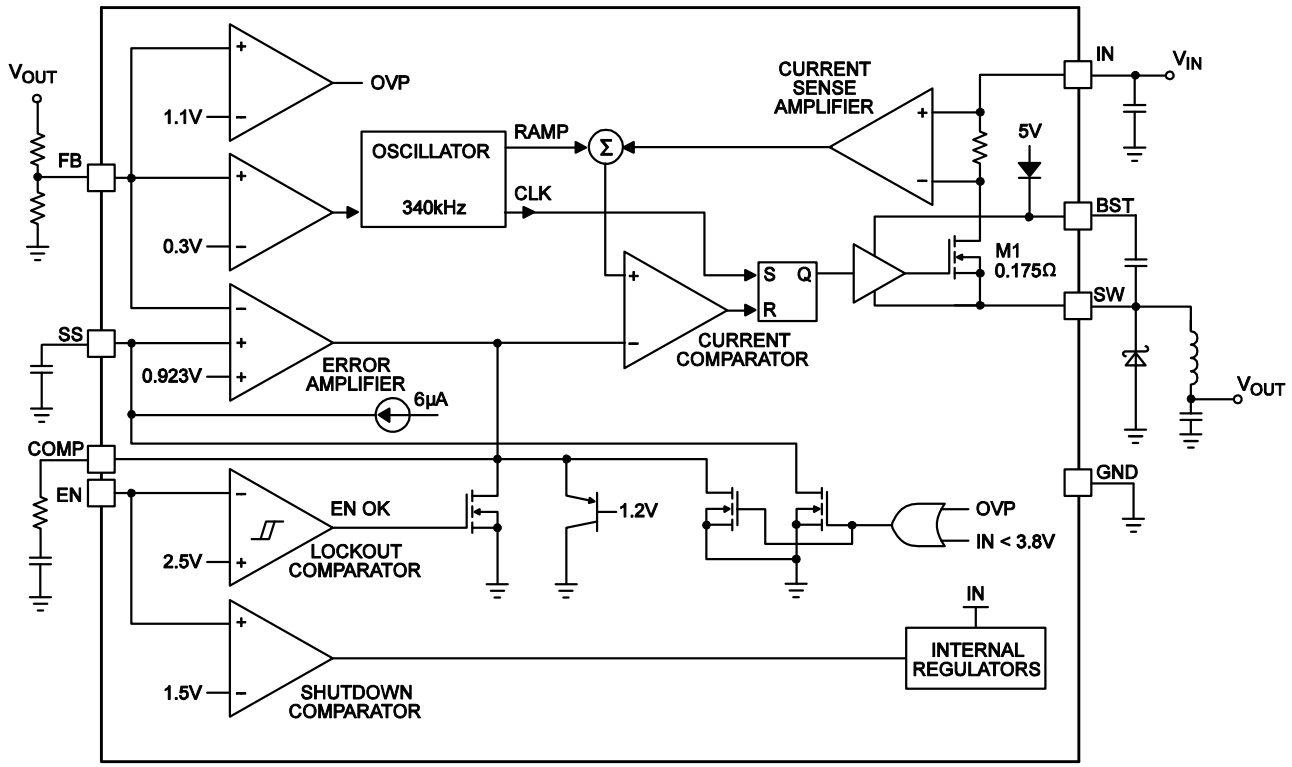


Figure 1: Functional Block Diagram

APPLICATION INFORMATION

Setting the Output Voltage

The output voltage is set using a resistive voltage divider from the output voltage to FB. The output voltage is divided down to the feedback voltage by the ratio shown in Equation (1):

$$V_{FB} = V_{OUT} \frac{R2}{R1+R2} \quad (1)$$

Where V_{FB} is the feedback voltage and V_{OUT} is the output voltage.

The output voltage can be calculated with Equation (2):

$$V_{OUT} = 0.923 \times \frac{R1+R2}{R2} \quad (2)$$

R2 can be as high as 100kΩ, but the typical value is 10kΩ. Using this typical value for R2, R1 can then be calculated with Equation (3):

$$R1 = 10.83 \times (V_{OUT} - 0.923) \ (k\Omega) \quad (3)$$

For example, for a 3.3V output voltage, R2 is 10kΩ, and R1 is 26.1kΩ.

Selecting the Inductor

An inductor is required to supply constant current to the output load while being driven by the switched input voltage. An inductor with a larger value results in less ripple current and lower output ripple voltage. However, an inductor with a larger value has a larger physical size, higher series resistance, and lower saturation current.

To select the inductance, allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum switch current limit. Ensure that the peak inductor current is below the maximum switch current limit. If a 0.45A load current is required, the inductance should be high enough to restrict the peak inductor current below 0.5A.

The inductance value can be calculated with Equation (4):

$$L = \frac{V_{OUT}}{f_S \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (4)$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, f_S is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that does not saturate under maximum inductor peak currents. The peak inductor current can be calculated with Equation (5):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (5)$$

Where I_{LOAD} is the load current.

Schottky Diode

When the high-side switch turns off, the current freewheels from the low-side external rectifier diode. To reduce the conduction loss of the external diode, a low forward voltage drop Schottky diode is strongly recommended.

Choose a diode with a maximum reverse voltage rating greater than the maximum input voltage and a current rating greater than the maximum load current. Table 1 lists example Schottky diodes and their manufacturers.

Table 1: Diode Selection Guide

Part Number	Voltage/Current Rating	Manufacturer
B130	30V, 1A	Diodes, Inc.
SL13	30V, 1A	Vishay, Inc.
MBRS130	30V, 1A	International Rectifier

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for best performance. Ceramic capacitors with X5R or X7R dielectrics are recommended, but tantalum or low ESR electrolytic capacitors are also sufficient.

Since the input capacitor (C1) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (6):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (6)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (7):

$$I_{C1} = I_{LOAD}/2 \quad (7)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (i.e.: 0.1μF) placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple for low ESR capacitors can be estimated with Equation (8):

$$\Delta V_{IN} = \frac{I_{LOAD}}{C1 \times f_S} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

Where C1 is the input capacitance value.

Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are recommended to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (9)$$

Where C2 is the output capacitance value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

With ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (11)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP9472 can be optimized for a wide range of capacitance and ESR values.

Compensation Components

The MP9472 employs current-mode control for easy compensation and fast transient response. The system stability and transient response are controlled through COMP. COMP is the output of the internal transconductance error amplifier. A series resistor-capacitor combination sets a pole-zero combination to control the characteristics of the control system.

The DC gain of the voltage feedback loop can be calculated with Equation (12):

$$A_{VDC} = R_{LOAD} \times G_{CS} \times A_{EA} \times \frac{V_{FB}}{V_{OUT}} \quad (12)$$

Where A_{VEA} is the error amplifier voltage gain, G_{CS} is the current sense transconductance, and R_{LOAD} is the load resistor value.

The system has two important poles. One is due to the compensation capacitor (C3) and the output resistor of the error amplifier, and the other is due to the output capacitor and the load resistor. These poles are determined with Equation (13) and Equation (14):

$$f_{P1} = \frac{G_{EA}}{2\pi \times C3 \times A_{VEA}} \quad (13)$$

$$f_{P2} = \frac{1}{2\pi \times C2 \times R_{LOAD}} \quad (14)$$

Where G_{EA} is the error amplifier transconductance.

The system has one important zero due to the compensation capacitor (C3) and the compensation resistor (R3). This zero can be determined with Equation (15):

$$f_{Z1} = \frac{1}{2\pi \times C3 \times R3} \quad (15)$$

The system may have another zero if the output capacitor has a large capacitance or a high ESR value. This zero is due to the ESR and capacitance of the output capacitor and can be determined with Equation (16):

$$f_{ESR} = \frac{1}{2\pi \times C2 \times R_{ESR}} \quad (16)$$

In this case, a third pole set by the compensation capacitor (C_{POLE}, from COMP to GND) and the compensation resistor (R3) is used to compensate for the effect of the ESR zero on the loop gain. This pole can be determined with Equation (17):

$$f_{P3} = \frac{1}{2\pi \times C_{POLE} \times R3} \quad (17)$$

The goal of the compensation design is to shape the converter transfer function to obtain a desired loop gain. The system crossover frequency where the feedback loop has unity gain is important. Lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies can cause system instability. It is recommended to set the crossover frequency below one-tenth of the switching frequency.

To optimize the compensation components, the following procedure can be used.

1. Choose the compensation resistor (R3) to set the desired crossover frequency. R3 can be determined with Equation (18):

$$R3 = \frac{2\pi \times C2 \times f_C}{G_{EA} \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}} < \frac{2\pi \times C2 \times 0.1 \times f_S}{G_{EA} \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}} \quad (18)$$

   Where f_C is the desired crossover frequency, typically below one-tenth of the switching frequency.

2. Choose the compensation capacitor (C3) to achieve the desired phase margin. For applications with typical inductor values, setting the compensation zero (f_{Z1}) below one-fourth of the crossover frequency provides sufficient phase margin.

   Determine the C3 value with Equation (19):

$$C3 > \frac{4}{2\pi \times R3 \times f_C} \quad (19)$$

   Where R3 is the compensation resistor.

3. Determine if a second compensation capacitor (C_{POLE}, from COMP to GND) is required. It is required if the frequency of the zero created by the ESR of the output capacitor is less than half of the switching frequency. Otherwise, Equation (20) is valid:

$$\frac{1}{2\pi \times C2 \times R_{ESR}} < \frac{f_S}{2} \quad (20)$$

   If this is the case, then add a second compensation capacitor (C_{POLE}) to set the pole (f_{P3}) at the location of the ESR zero. Determine the C_{POLE} value with Equation (21):

$$C_{POLE} = \frac{C2 \times R_{ESR}}{R3} \quad (21)$$

External Bootstrap Diode

An external bootstrap diode may enhance the efficiency of the regulator and is required under the following conditions:

- V_{OUT} = 5V or 3.3V
- Duty cycle is high: $D = \frac{V_{OUT}}{V_{IN}} > 65\%$

In these cases, an external BST diode is recommended from the output of the voltage regulator to BST (see Figure 2).

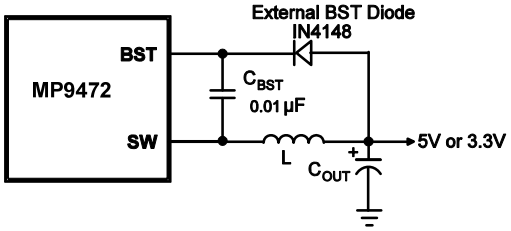


Figure 2: Optional External Bootstrap Diode Added to Enhance Efficiency

The recommended external BST diode is IN4148, and the recommended BST cap is 0.01µF.

The MP9472 charges the BST capacitor through an internal 5V power supply. During each period, it pulls SW to GND internally to charge the BST capacitor. In light-load mode, if SW cannot be pulled down to GND and charge the BST voltage high enough, even when the duty cycle is low and the external bootstrap diode is added, avoid running the MP9472 in extremely light loads or adding a dummy load to keep it in normal operation.

TYPICAL APPLICATION CIRCUIT

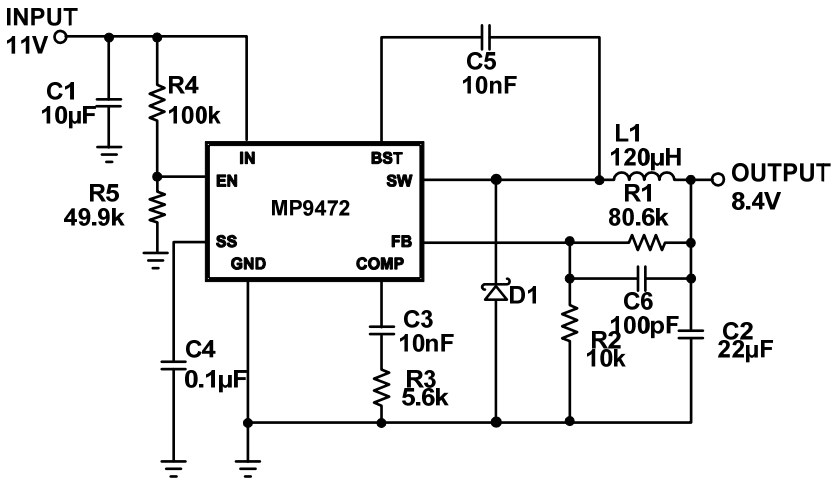
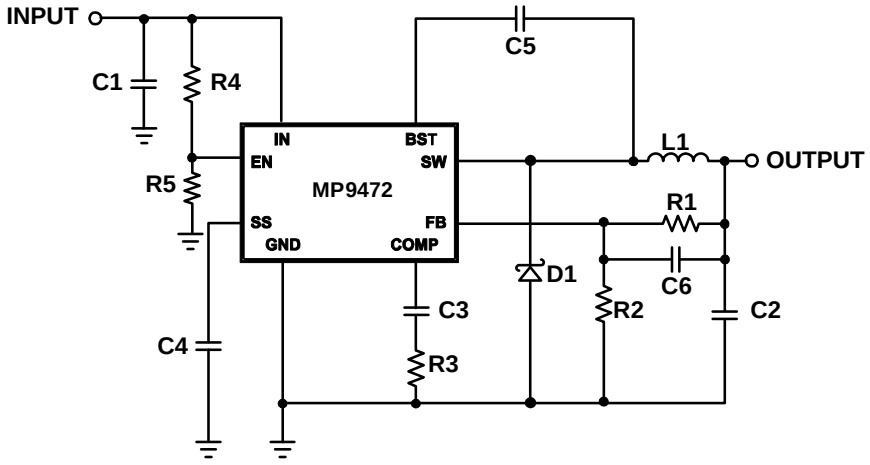


Figure 3: MP9472 with 8.4V Output, 22µF Ceramic Output Capacitor

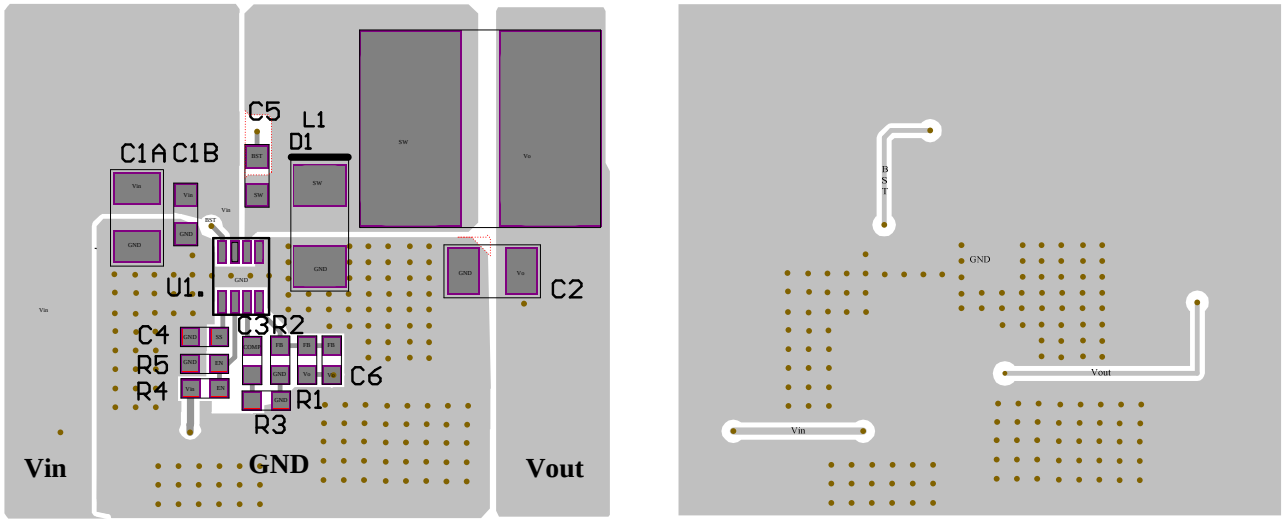
PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 4 and follow the guidelines below.

1. Keep the path of switching current short and minimize the loop area formed by input cap, high-side MOSFET, and low-side rectifier diode.
2. Place the ceramic bypass capacitors close to V_{IN}.
3. Keep all feedback connections short and direct.
4. Place the feedback resistors and compensation components as close to the chip as possible.
5. Route SW away from sensitive analog areas such as FB.
6. Connect IN, SW, and especially GND to a large copper area to cool the chip to improve thermal performance and long-term reliability.



MP9472 Typical Application Circuit

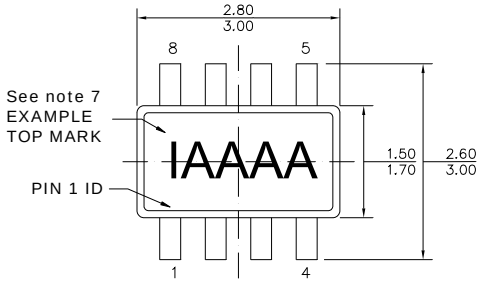


Top Layer **Bottom Layer**

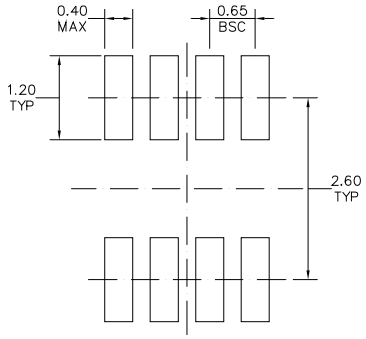
Figure 4: MP9472 Typical Application Circuit and PCB Layout Guide

PACKAGE INFORMATION

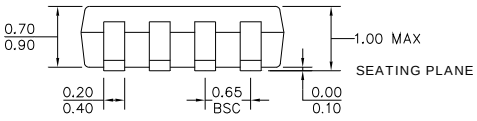
TSOT23-8



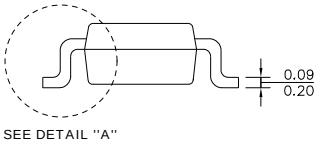
TOP VIEW



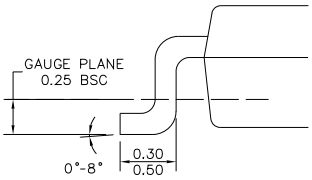
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-193, VARIATION BA.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)