Application Note for Peak-Power Design with Optimized Power Loss and Transformer Size for the HFC0300

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ABSTRACT

Applications—including printers, data-storage equipment, audio amplifiers and motor drivers—usually require power supplies that deliver high peak-to-nominal load ratios. The HFC0300 is a variable off-time controller optimized for these applications. This application note introduces the operating principles and features of HFC0300 for delivering peak load, and outlines an optimized peak-power design method that lowers power loss and minimizes transformer size. Finally, this application note provides a detailed step-by-step design example with peak load profile, which includes both theoretical calculations and experimental verification.

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1. INTRODUCTION

Peak power is defined as the amount of energy that exceeds the nominal rating for short specified durations (typically tens of milliseconds and up to seconds at the most).[1] Many applications require power supplies that can deliver high peak-to-nominal load ratios due to high start-up currents or sudden short-duration heavy loads. Therefore, a good alternative power controller allows the power system to deal with the worst-case short-duration peak current while providing good operating performance at nominal load. The HFC0300 is a power conversion IC with intelligent peak-power management technology that enables the system to stay within peak power constraints. The device also provides significant size and cost savings.

This application note is intended for engineers designing AC-DC flyback power supplies using the HFC0300 for peak power applications. This note provides guidelines to help the engineer to quickly select key components and also complete a suitable transformer design.

2. HFC0300'S PEAK-POWER FEATURES

HFC0300 is a variable off-time controller that uses an external capacitor connected to the FSET pin to set the frequency. It can also boost its frequency with increased loads.

The variable off-time control scheme offers various advantages over traditional PWM-controlled power supplies. For instance, the feedback signal can boost the primary-side switching frequency and increase the current-limit threshold to transfer energy as appropriate to the load conditions to the power output. Since variable off time control only initiates a switching cycle when the system requires an energy transfer, the effective-average switching frequency under light-load conditions is much lower, which benefits efficiency performance. When the output power falls below a given level, the controller enters burst mode to further reduce the power loss at no load or light load condition. Figure 1 shows frequency variation against the COMP voltage. [2]

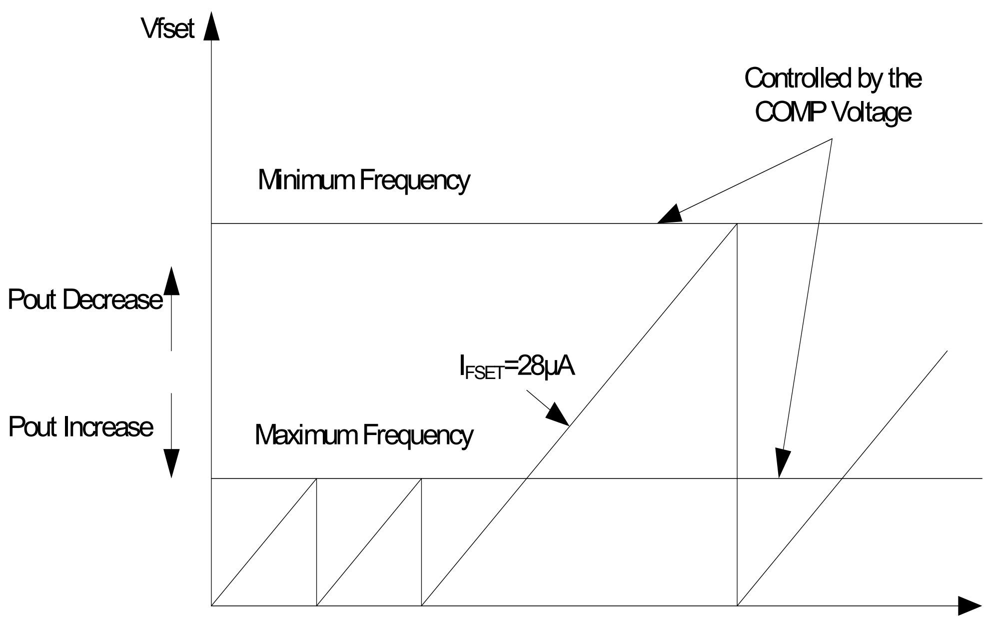

Figure 1: COMP Voltage as a Function of the Switching Frequency

Additionally, reducing the frequency results in the peak current decreasing with the load to protect the transformer against mechanical resonance. Figure 2 shows the peak current vs. COMP voltage curve. The COMP voltage ranges from 0.9V to 3.2V. Peak current decreases when COMP voltage exceeds 2.1V. The part stops switching when the COMP voltage increases over the 3.2V threshold and resumes switching when the COMP voltage falls below the 3.1V threshold.

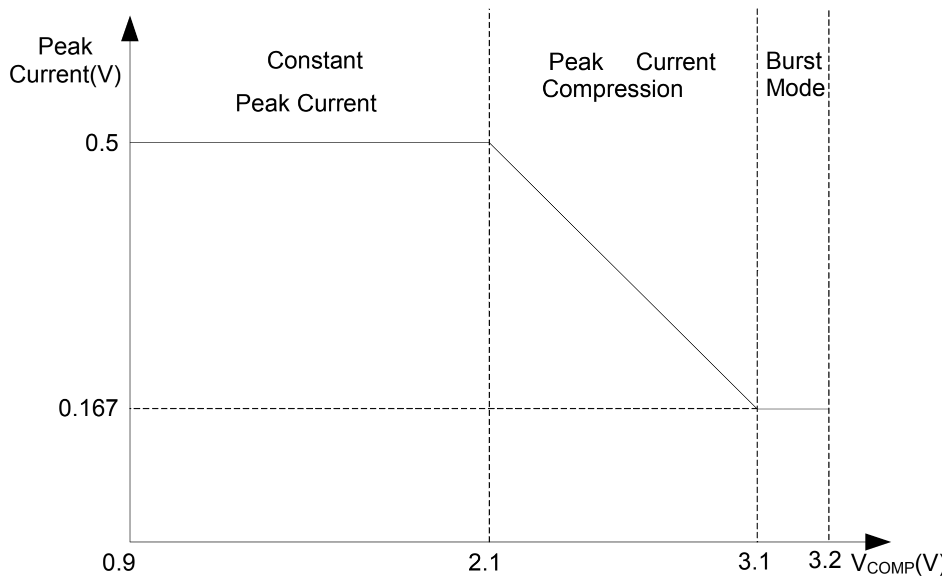

Figure 2: Peak Current vs. COMP Voltage

In addition, the HFC0300 integrates a variety of protection features to minimize the external component count, such as internal V_{CC} Under-Voltage Lockout (UVLO), Over-Load Protection (OLP), Over-Voltage Protection (OVP), Short-Circuit Protection (SCP), and Thermal Shutdown (TSD).

The HFC0300 adjusts the output power by changing the frequency where peak power occurs at the maximum frequency. The COMP voltage drops to its bottom value at the meantime.

Figure 3 plots the average switching frequency of a 60W nominal load using a 90W peak-load power supply with a low-line input (90V) and various distinct load conditions.

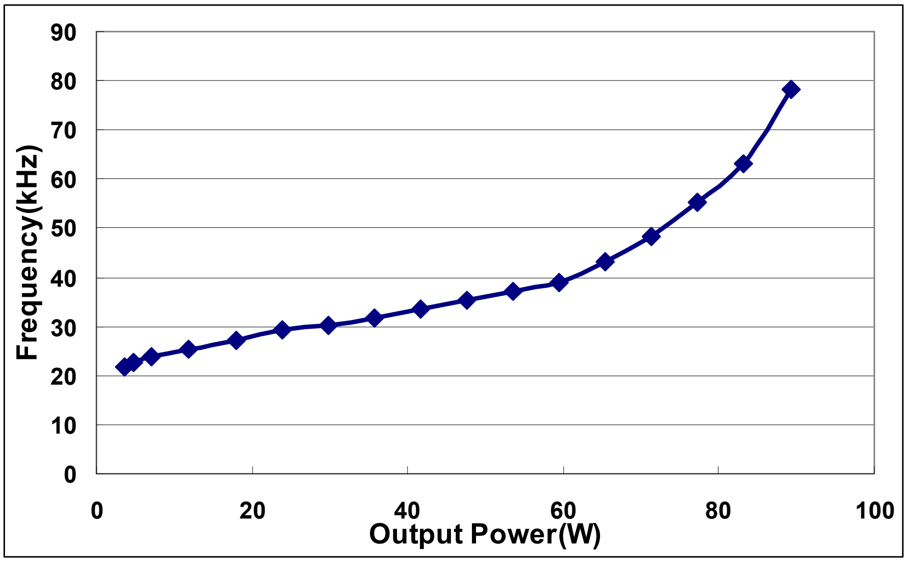

Figure 3: Switching Frequency vs. Output Power

The frequency can go as high as 80kHz at a 90W extreme peak load, and can go as low as 40kHz at a 60W nominal load, and drop further to 28kHz at half the nominal load.

The high frequency under peak load conditions allows a minimal transformer core size. Therefore, for the HFC0300, the core size can be chosen for the nominal load condition to meet the thermal requirement, since the peak current is already at its maximum value under this condition. Consequently the increase in effective-switching frequency at peak load does not increase the core-flux density. On the contrary, traditional PWM controlled power supplies typically run at a fixed frequency of only 40kHz or less over the entire load range up to the maximum peak load. Therefore the transformer core size must be selected for the peak load condition to avoid saturation when the primary current increases to satisfy the peak load requirement. [3]

3. DESIGN METHOD FOR PEAK POWER

3.1 Current Solution

The traditional design method initially determines the converter operation mode, such as CCM, BCM or DCM given low line input and peak load conditions. Then select the primary peak current and primary inductance accordingly. This kind of circuit delivers a much higher peak power than needed, which results in cost over-runs and big core sizes of the magnetic components because this method treats the peak power as continuous maximum power. However, the application only demands peak power for very short periods due to start up or a heavy pulse load. Typical peak-to-nominal ratio is usually $P_{PEAK} \geq 1.5P_{CONT.}$, depending on the load configuration.

The HFC0300's high switching frequency allows for a smaller core to deliver the peak power, but the short duration prevents the transformer windings from overheating and reduces the heatsink requirements. If necessary, select a smaller transformer to reduce the winding current density. Ultimately, these features contribute to the HFC0300's optimal use in applications that demand short duration, high-peak power, and low nominal power.

3.2 Optimized Design Introduction

An optimized design procedure requires specified peak and nominal powers. The peak power contributes to electrical stress, which is a deciding factor in selecting the device, while the nominal power determines the RMS rating selection. Take both peak power and nominal power into consideration when designing the transformer for power delivery at the minimum input line voltage—this may optimize the transformer and heatsink sizes. Furthermore, the optimization method in this application note also takes efficiency at nominal power into consideration.

This section presents a design procedure as per the schematic of Figure 4. The peak power for the HFC0300 must be guaranteed when the frequency reaches its maximum value in any operation mode. From Figure 2, the following equation determines the switching frequency range based on C_{FSET} and COMP voltage range.

$$f_S = \frac{1}{\frac{C_{FSET} \times V_{COMP}}{28} + 0.6\mu s} \tag{1}$$

The maximum frequency corresponds to 0.9V minimum COMP voltage and the minimum frequency corresponds to 3.1V maximum COMP voltage, which are constant values once the capacitor connected to the FSET pin is given.

$$f_{S-MAX} = \frac{1}{\frac{C_{FSET} \times 0.9V}{28} + 0.6\mu s} \tag{2}$$

$$f_{S-MIN} = \frac{1}{\frac{C_{FSET} \times 3.1V}{28} + 0.6\mu s} \tag{3}$$

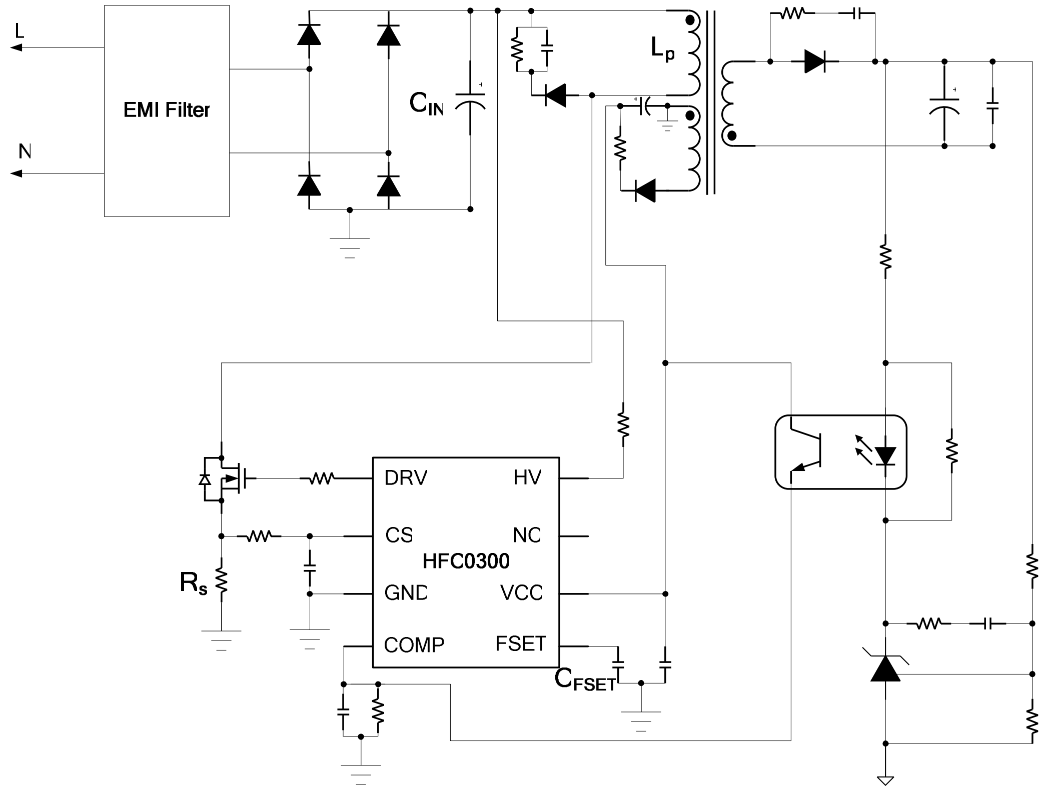

Figure 4: Typical Application

Usually, each specification has a pre-determined frequency range for nominal and peak load. The design target is to achieve the required peak power and good performance at nominal power.

Equations (4) and (5) describe the power delivered by the power supply:

In DCM mode:

$$P_{DCM} = \frac{1}{2} L_P I_P{}^2 f_S \tag{4}$$

In CCM mode:

$$P_{CCM} = \frac{V_{DC(MIN)} NV_O}{V_{DC(MIN)} + NV_O} I_p - \frac{1}{2 f_S L_P} \left(\frac{V_{DC(MIN)} NV_O}{V_{DC(MIN)} + NV_O}\right)^2 \tag{5}$$

Based on Figure 2, the peak current is

$$I_P = \begin{cases} \dfrac{0.5}{R_S} & V_{COMP} \le 2.1 \\ \dfrac{1.1993 - 0.333 V_{COMP}}{R_S} & 2.1 < V_{COMP} \le 3.1 \end{cases} \tag{6}$$

Where:

- L_P is the primary inductance,
- I_P is the primary peak current,
- $V_{DC(MIN)}$ is the minimum input DC voltage,
- V_O is the output set voltage,
- N is the turns ratio (primary/secondary),
- R_S is the current-sense resistance,
- V_{COMP} is the COMP voltage.

Substituting f_S with $f_{S\text{-}MAX}$ can get the peak power values $P_{PEAK\text{-}DCM}$ and $P_{PEAK\text{-}CCM}$.

Basically, $V_{DC(min)}$ is determined by the AC input voltage and input capacitors, N is determined by the trade off between primary MOSFET's and secondary Schottky diode's voltage ratings. The other parameters are pre-determined, leaving L_P and R_S as the remaining key parameters in the power system design. However, given the numerous combinations of L_P and R_s that can deliver the required peak power for a given maximum-frequency condition, selecting appropriate L_P and R_S values must account for the required peak power, good performance at nominal load, while minimizing cost and size.

3.3 Optimized Design Flow

A. Predetermined Input and Output Specifications

Determine the following input and output specifications first when designing a power supply with peak power profile:

- Input AC voltage range, $V_{AC(MIN)}$, $V_{AC(MAX)}$: for example $90V_{AC}$ to $265V_{AC}$
- Input AC frequency, f: for example f=50Hz
- Output voltage and nominal/peak output power, V_O, P_{NOM}, P_{PEAK}: for example V_O=24V, P_{NOM}=60W, P_{PEAK}=90W
- Estimated efficiency, η: for example η=85%

Estimate the power conversion efficiency to calculate the required input power. With the estimated efficiency, the nominal input power is:

$$P_{IN} = \frac{P_{NOM}}{\eta} \tag{7}$$

B. Determine Input Capacitor and DC Bus Voltage Range

Typically, select the input capacitor (C_{IN}) at around 1.5µF to 2µF per watt of input power. With the input capacitor chosen, the minimum input capacitor voltage at nominal load condition is obtained as:

$$V_{DC(MIN)} = \sqrt{2(V_{AC(MIN)})^2 - \frac{2P_{IN}}{C_{IN}}\tau_1} \tag{8}$$

Where τ_1 is the input capacitor discharging time per cycle as shown in Figure 5.

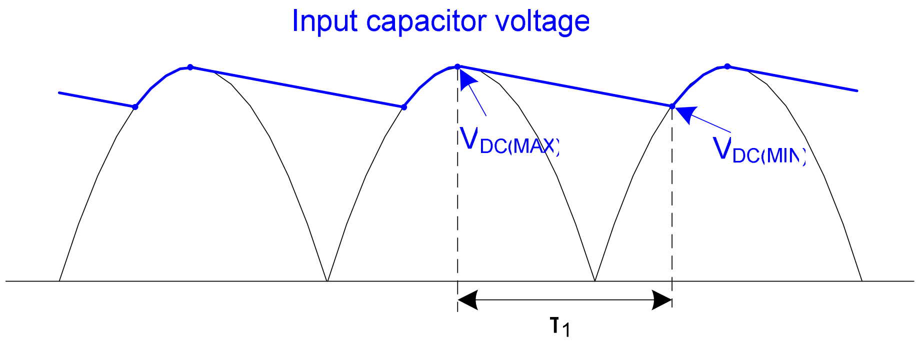

Figure 5: Input Capacitor Voltage Waveform

The maximum input capacitor voltage is given as:

$$V_{DC(MAX)} = \sqrt{2}V_{AC(MAX)} \tag{9}$$

C. Duty Cycle, Turns Ratio and C_{FSET} Selection

When the MOSFET is OFF, the input voltage (V_{DC}) and the output voltage reflected on the primary side, appear across the MOSFET, as shown in Figure 6.

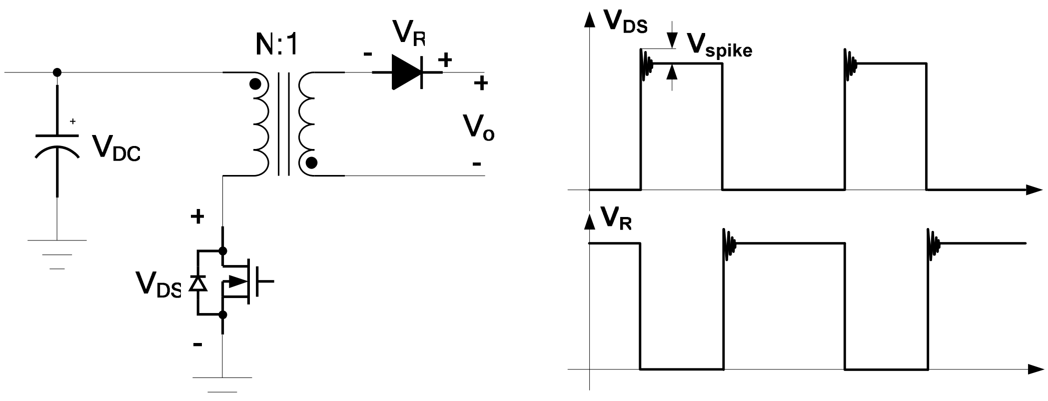

Figure 6: Voltage Stress of Primary MOSFET and Secondary Rectifier Diode

The maximum MOSFET voltage (V_{DS}) is then:

$$V_{DS} = \frac{V_{DC(MAX)} + N(V_O + V_F) + V_{SPIKE-MOSFET}}{k} \tag{10}$$

Where V_F is the rectifier diode's forward voltage, k is the derating factor (typically 0.9), and $V_{SPIKE-MOSFET}$ is produced by the transformer's primary leakage inductance and is typically around 60V.

When the MOSFET turns on, the output voltage (V_O) and the input voltage reflected on the secondary winding appear across the diode. The maximum diode voltage (V_R) is then:

$$V_R = \frac{\frac{V_{DC(MAX)}}{N} + V_O + V_{SPIKE-DIODE}}{k} \tag{11}$$

Where the secondary parasitic inductance and capacitance causes $V_{SPIKE\text{-}DIODE}$, which is typically around 20V. With a low-line input voltage and nominal load condition, the controller enters CCM. The maximum duty cycle is:

$$D_{MAX} = \frac{N(V_O + V_F)}{V_{DC(MIN)} + N(V_O + V_F)} \tag{12}$$

Based on equations (10) and (11), reducing N reduces the voltage stress across the MOSFET, but increases the voltage stress on the secondary-side rectifier diode. Therefore, the value of N is a trade-off between MOSFET's and diode's voltage stresses. In addition, select a maximum duty cycle below 0.5 in order to avoid sub-harmonic oscillation that can limit N's range.

HFC0300 has Over-Load Protection (OLP) with a delay time relative to C_{FSET}:

$$\tau_{DELAY} = 74ms \times \frac{C_{FSET}}{330pF} \tag{13}$$

A very small C_{FSET} can trigger the OLP before completing start-up under heavy-load conditions, so determine C_{FSET} according to the load condition. In addition, keep the minimum frequency ($f_{S\text{-}MIN}$) above 20kHz to avoid audible noise—select C_{FSET} less than 446pF as per equation (3).

D. Combinations of L_P and R_S for a Required Peak Power

As described in section 3.2 Optimized Design Introduction there are multiple L_P and R_S combinations that can deliver the required peak power for a given maximum frequency (pre-determined by C_{FSET}). For a given peak power, determining L_P ultimately determines R_S. The following example is based on the following conditions: (except L_P, actual applications either provide the other parameters, or they can be calculated based on the previous-discussed design flow).

- L_P=200µH,
- $V_{DC(MIN)}$=95V,
- V_O=24V,
- P_{NOM}=60W,
- P_{PEAK}=90W,
- η=85%,
- N=3,
- C_{FSET}=330pF,
- C_{IN}=150µF

For a given maximum frequency, different R_S values result in different operating modes and deliver different peak power values.

First, determine the operating mode (DCM or CCM) for a given R_S. Then, calculate the peak power. Following calculations can determine the operation mode for a given R_S.

Given, $P_{PEAK\text{-}DCM}=P_{PEAK\text{-}CCM}$ (from equations (4) and (5) with $f_S=f_{S\text{-}MAX}$), the root R_{BCM}=0.228Ω.

When $R_S<R_{BCM}$, the HFC0300 works in CCM; when $R_S=R_{BCM}$, it works in BCM; and when $R_S>R_{BCM}$, it enters DCM. Equation (14) describes the relationship between P_{PEAK} and R_S, and Figure 7 shows the curve.

$$P_{PEAK} = \begin{cases} P_{PEAK-DCM} & R_S \geq R_{BCM} \\ P_{PEAK-CCM} & R_S < R_{BCM} \end{cases} \tag{14}$$

Figure 7 shows clearly that a lower R_S results in a higher P_{PEAK}. At the same time, the operating mode switches from DCM to CCM when R_S decreases. This example works in CCM at 90W peak power, resulting in R_S=0.152Ω from equation (14). So, L_P=200µH and R_S=0.152Ω can deliver 90W peak power at the maximum frequency.

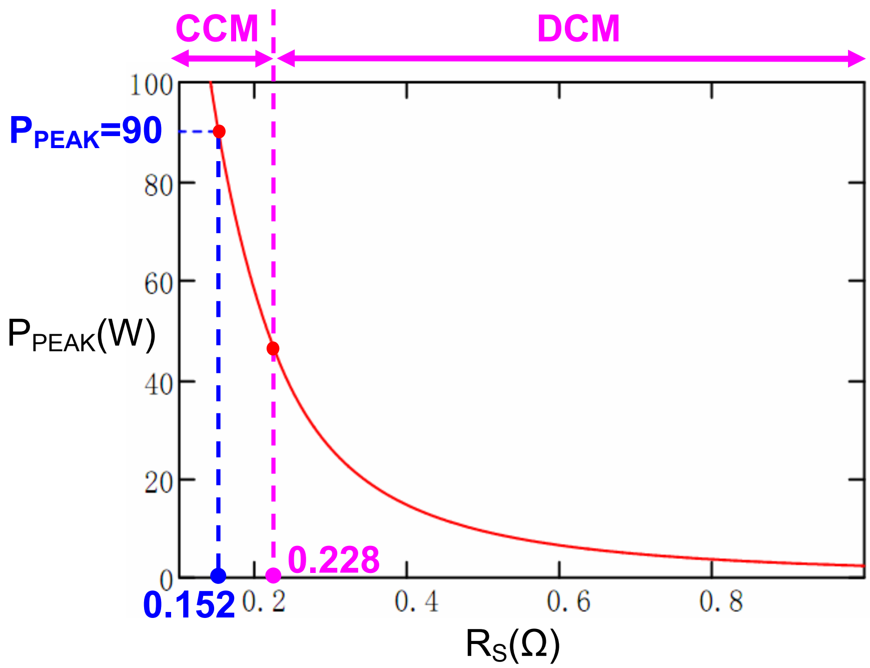

Figure 7: Peak Power vs. Sense Resistor

E. Output Power Calculation within the COMP Voltage Range

Apart from achieving the peak power, the nominal power also figures into design optimization. For a given L_P and R_S pair, various COMP voltage results in different output power levels and operation modes. Finding the root from P_{DCM}=P_{CCM} with given L_P=200µH, R_S=0.152Ω and C_{FEST}=330pF, then $V_{COMP-BCM}$=1.349V is obtained.

If V_{COMP}<$V_{COMP-BCM}$, HFC0300 works in CCM; for V_{COMP}=$V_{COMP-BCM}$, it works in BCM; while for V_{COMP}>$V_{COMP-BCM}$, it is in DCM. Therefore, a 60W nominal load works in DCM mode while 90W peak load in CCM mode.

Figure 8 shows the curve of the output power vs. COMP voltage for L_P=200µH, R_S=0.152Ω and C_{FSET}=330pF.

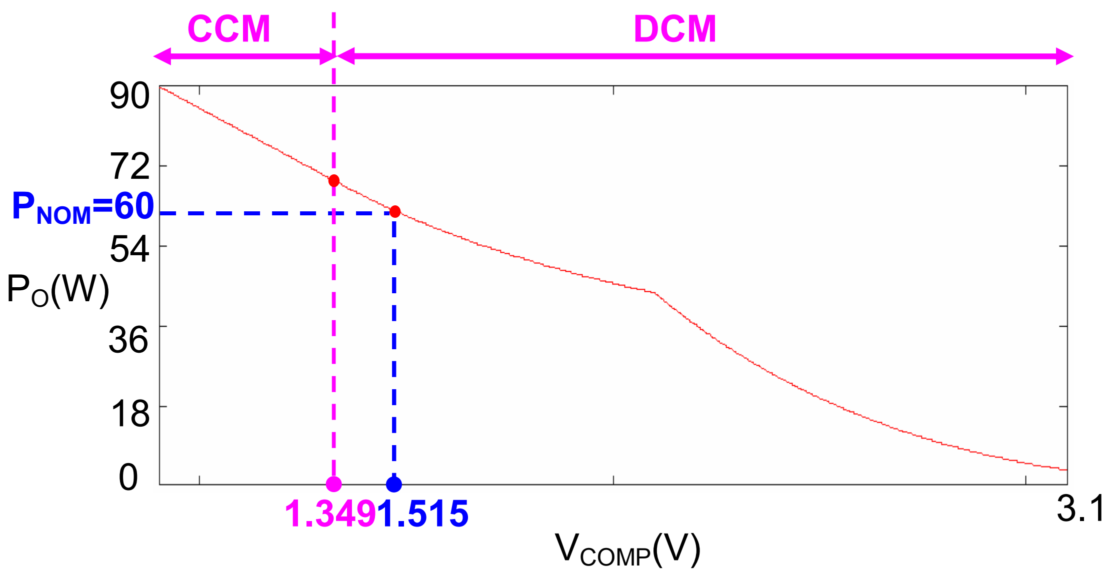

Figure 8: Output Power vs. COMP Voltage (L_P=200µH R_S=0.152Ω)

For a given L_P, use the aforementioned calculation method to estimate the corresponding R_S. Table 1 shows the various R_S values for a given L_P and the operation mode for the both peak and nominal loads:

Table 1: Combinations of L_P and R_S for 90W Peak Power

L_P(µH)	R_S(Ω)	Operation Mode @ P_{NOM}=60W	Operation Mode @ P_{PEAK}=90W	Curve # from Figure 9
100	0.114	DCM	BCM	#1
200	0.152	DCM	CCM	#2
300	0.171	BCM	CCM	#3
400	0.182	CCM	CCM	#4
500	0.19	CCM	CCM	#5
600	0.195	CCM	CCM	#6
700	0.199	CCM	CCM	#7
800	0.202	CCM	CCM	#8

Figure 9 shows the output power vs. COMP voltage curves for the various combinations of L_P and R_S.

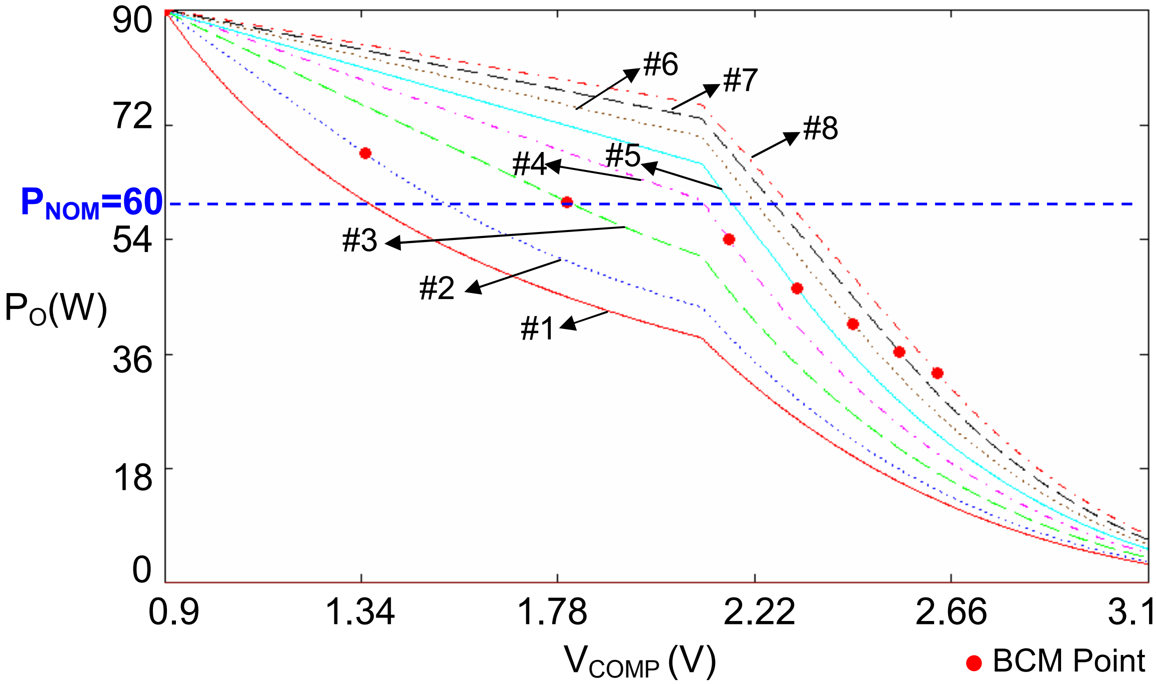

Figure 9: Output Power vs. COMP Voltage for Various L_P and R_S

F. Estimating Transformer Size and Power Loss

Although the listed combinations of L_P and R_S can deliver the required peak power, the transformer size and the power loss are not be optimized. The goal of the design is to get the optimized solution with both a small transformer for peak power delievery and low power loss at nominal load.

■ Transformer Core Size Calculation

Based on the AP rule for transformer core size calculation, estimate the core size with equation (15):

$$T_{size} = \frac{L_P I_P I_{PRMS}}{B_{MAX} K_J K_U} = \frac{L_P I_{PRMS}}{2B_{MAX} R_S K_J K_U} \tag{15}$$

Here, R_S determines the peak current by equation (6), where:

- B_{MAX} is the maximum-allowed flux density, which is usually 0.3T,
- K_J is the current-density coefficient, usually 450A/cm^2,
- K_U is winding factor, which is 0.2,
- I_{PRMS} is the primary RMS current which can be simplified as a constant value (1.1A under 60W nominal load condition—verified by calculation that the RMS current varies little and thus has little impact on core size).

■ Power Loss Calculation (Electrical)

The power loss is comprised of several parts (electrical only—magnetic loss not yet specified due to undetermined core size, type and material): the MOSFET conduction loss, the MOSFET turn-on loss, the MOSFET turn off loss, and the secondary-diode conduction loss.

MOSFET Conduction Loss:

$$P_{MOS-CON-DCM} = f_s \int_0^{\frac{L_P I_P}{V_{DC(MIN)}}} (\frac{V_{DC(MIN)} t}{L_P})^2 R_{DS} dt \quad \text{(DCM mode) (16)}$$

$$P_{MOS-CON-CCM} = f_S \int_0^{\frac{D}{f_S}} (I_P - \frac{V_{DC(MIN)} D}{L_P f_S} + \frac{V_{DC(MIN)} t}{L_P})^2 R_{DS} dt \quad \text{(CCM mode) (17)}$$

Where R_{DS} is the ON resistance of the primary MOSFET.

MOSFET Turn-On Loss:

$$P_{MOS-ON-DCM} = 0 \quad \text{(DCM mode) (18)}$$

$$P_{MOS-ON-CCM} = \frac{(V_{DC(MIN)} + NV_O)(I_P - \frac{V_{DC(MIN)} D}{L_P f_S}) \tau_{CROSS\_ON} f_S}{6} \quad \text{(CCM mode) (19)}$$

Where $\tau_{CROSS-ON}$ is the overlapping time between the MOSFET voltage and current when it turns on.

MOSFET Turn-Off Loss:

$$P_{MOS-OFF} = \frac{(V_{DC(MIN)} + NV_O) I_P \tau_{CROSS-OFF} f_S}{6} \quad (20)$$

Where $\tau_{CROSS-OFF}$ is the overlapping time between the MOSFET voltage and current when it turns off.

Diode conduction loss:

$$P_{Diode-CON-DCM} = f_S \int_0^{\frac{L_P I_P}{NV_O}} V_{DIODE} (NI_P - \frac{N^2 V_O}{L_P} t) dt \quad \text{(DCM mode) (21)}$$

$$P_{Diode-CON-CCM} = f_S \int_0^{\frac{1-D}{f_S}} V_{DIODE} (NI_P - \frac{N^2 V_O}{L_P} t) dt \quad \text{(CCM mode) (22)}$$

Where V_{DIODE} is the diode forward voltage drop. The total electrical power loss is the sum of the resulting values from the previous equations.

Based on equations (15)-(22), calculate the transformer size and electrical power loss for various combinations of L_P and R_S. Figure 10 shows the plot of the final result .

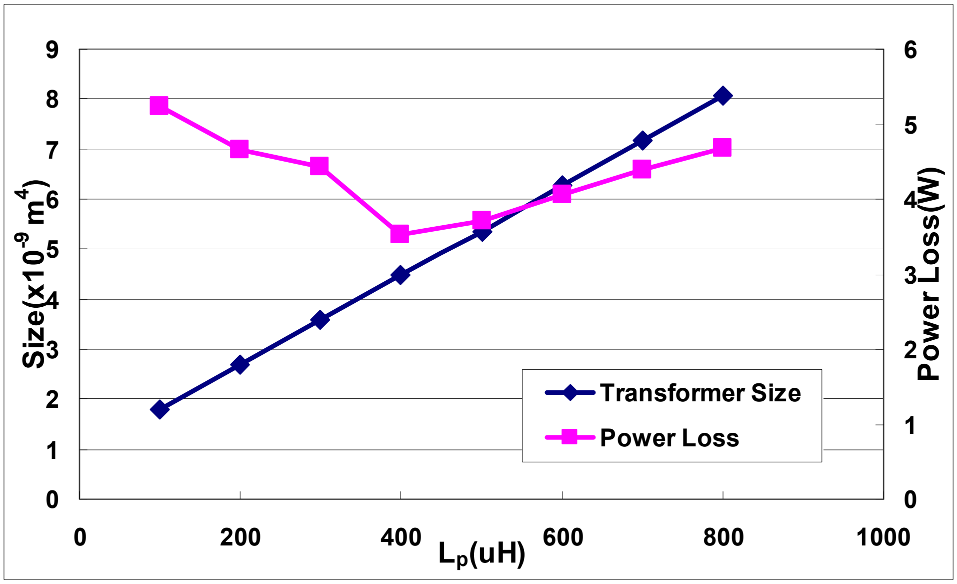

Figure 10: Transformer Size and Power Loss (Electrical) vs. L_P

The curves show that lower L_P results in smaller transformer. However, reducing the electrical power loss involves an optimized range of L_P. The transformer size and power loss curve in Figure 10 shows that the best combination is L_P=400µH and R_S=0.18Ω (Choose the closest values in practice if the inductance and resistance values are not available) for an appropriate trade-off between power loss and transformer size.

G. Transformer Design

The last step is to design the transformer based on the selected L_P and R_S values. The core area product (A_EA_W) is the core magnetic cross-section area multiplied by the available winding window area, and can estimate the core size for a given application. The following is a rough estimate of A_EA_W(cm^4) is:[4]

$$A_EA_W = \frac{L_P I_P I_{PRMS}}{B_{MAX} K_J K_U} \tag{23}$$

Where I_{PRMS} is the primary RMS current under a 60W nominal load condition:

$$I_{PRMS} = \sqrt{\left[(\frac{I_P + I_{valley}}{2})^2 + \frac{1}{12}(I_P - I_{valley})^2\right] D} \tag{24}$$

In this example, A_EA_W is around 4.82x10^{-9}m^4 based on equation (23). For traditional PWM control with a 40kHz fixed frequency (choose the HFC0300's nominal load frequency for comparison), a 1.15mH primary inductor could deliver the same peak power with the same peak-current condition based on equation (5), and A_EA_W is 1.45x10^{-8}m^4 based on equation (23)—which is nearly three times the HFC0300's optimized core size. Therefore, the transformer core size could be significantly reduced.

For a given core size, equation (25) defines the minimum value of primary turns (N_P) to prevent the core from saturating:

$$N_P = \frac{L_P I_P}{A_E B_{MAX}} \tag{25}$$

The number of secondary winding turns (N_S) is a function of N and N_P as per equation (26):

$$N_S = \frac{N_P}{N} \tag{26}$$

The winding loss depends on the RMS current value and the length and the cross-sectional area of the wire, so select it to minimize the winding conduction loss. The primary-side RMS current is given by equation (24), and the RMS current on secondary side is given by equation (27):

$$I_{SRMS} = N \times \sqrt{\left[(\frac{I_P + I_{valley}}{2})^2 + \frac{1}{12}(I_P - I_{valley})^2\right] D} \tag{27}$$

Then equations (28) and (29) provide the the primary- and secondary-side wire sizes:

$$S_{PRMS} = \frac{I_{PRMS}}{J} \tag{28}$$

$$S_{SRMS} = \frac{I_{SRMS}}{J} \tag{29}$$

Here, J is the wire current density, which is 450A/cm^2 typically.

Given the skin effect and proximity effect on the conductor, select a wire diameter of less than 2△d, where △d is the skin effect depth as determined by:

$$\Delta d = \sqrt{\frac{1}{\pi f_s \mu \sigma}} \times 10^3 (mm) \tag{30}$$

Where μ is the magnetic permeability of the conductor which is usually $4\pi x10^{-7}$H/m, σ is the conductive of the wire which is typically $6x10^7$S/m.

Based on the determined wire size, check the window coefficient (winding area/total window area) for a sufficient margin (basically the ratio is 0.1-0.2).

The following describes the transformer for this example:

N_P: N_S: N_{AUX}=50:15:8 with 400μH primary inductance. The core is EER28. The more detailed and specific wire structure is shown in Figure 11, Figure 12 and Table 2.

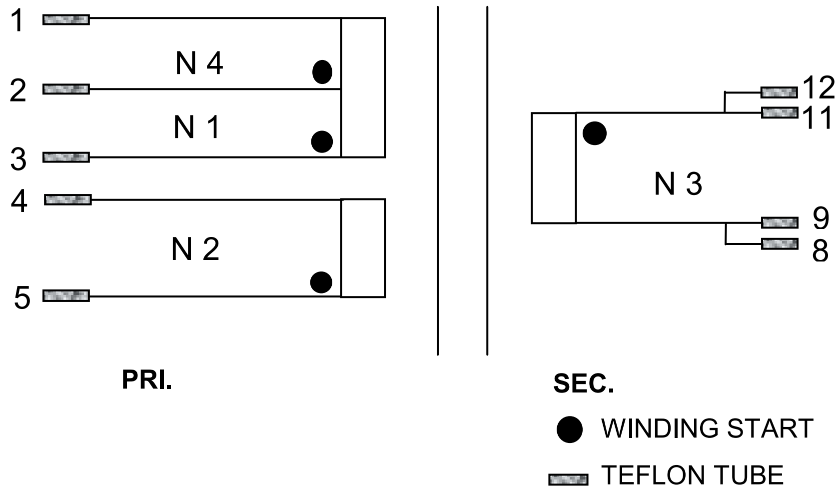

Figure 11: Connection Diagram

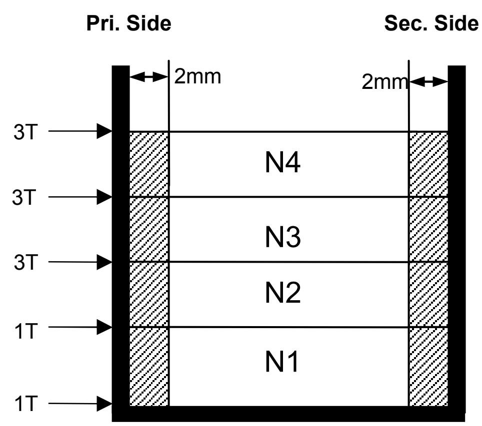

Figure 12: Winding Diagram

Table 2: Winding Order

Tape(T)	Winding	Edge Tape (Pri.)	Terminal (start-end)	Edge Tape (Sec.)	Wire Size (Φ)	Turns (N)
1						
	N1	2mm	3 → 2	2mm	0.33mm*2	25
1						
	N2	2mm	5 → 4	2mm	0.2mm*1	8
3						
	N3	2mm	11,12 → 8,9	2mm	0.33mm*7	15
3						
	N4	2mm	2 → 1	2mm	0.33mm*2	25
3						

4. EXPERIMENTAL VERIFICATION

To verify the design based on the procedure presented in this application note, we built and tested the circuit in Figure 13 for the given input/output conditions (Input: 90V_{AC} to 265V_{AC}; Output: 24V, nominal/peak load: 2.5A/3.75A).

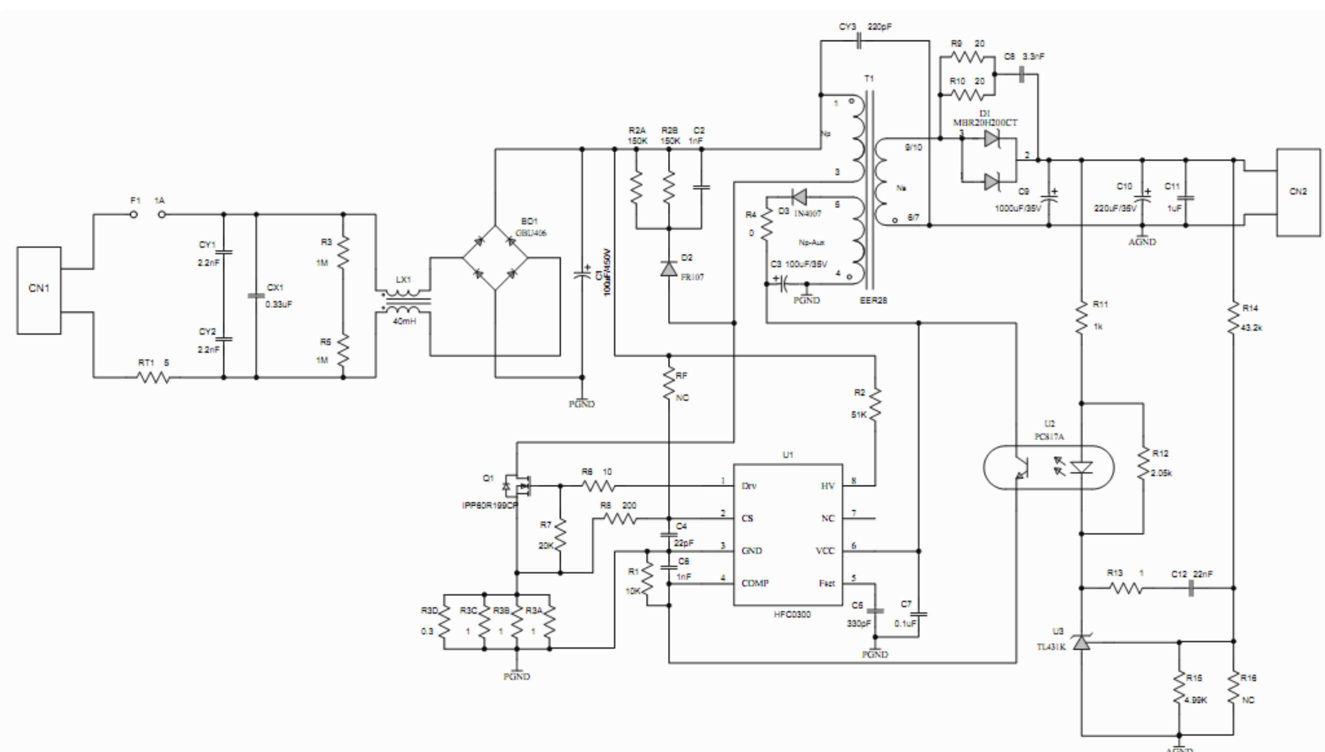

Figure 13:Schematic of 90W Peak Power Converter with HFC0300

4.1 Steady State

Figure 14 shows 60W nominal power with a low line input waveform:

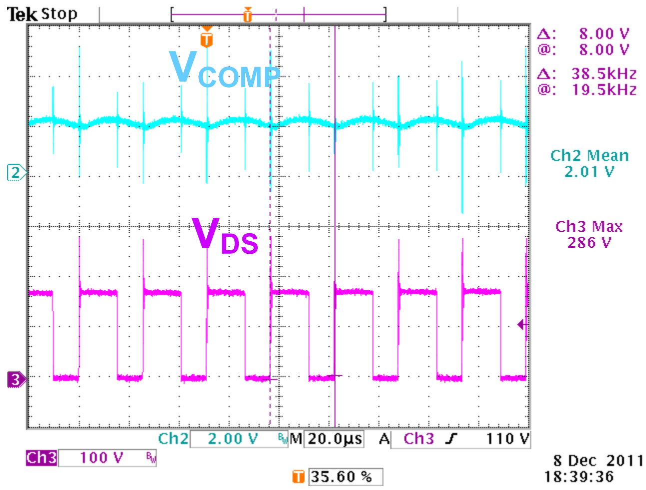

Figure 14: Norminal Load (60W) at Low Line Input (90V_{AC})

Figure 15 shows 90W peak power with a low line input waveform :

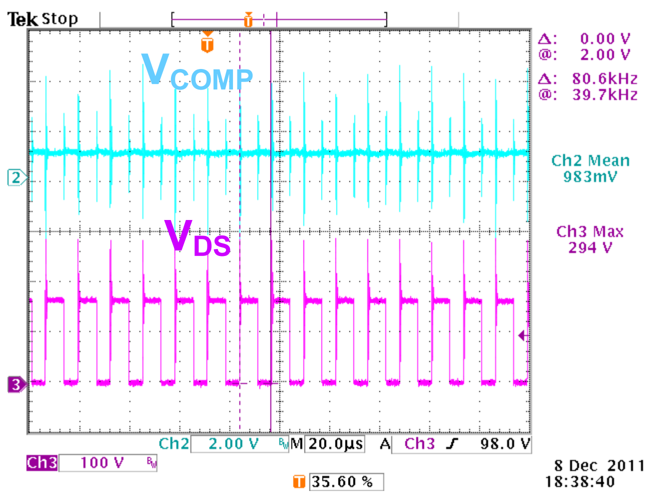

Figure 15: Peak Load (90W) at Low Line Input (90V_{AC})

Both are in CCM. As the load increases from 60W to 90W, the frequency increases from 39kHz to 80kHz, while the COMP voltage drops from 2.0V to 0.98V, which is very close to the 60W/90W points in curve 4 (L_p=400µH R_s=0.18Ω) in Figure 9. This experiment verifies the accuracy of the theoretical calculations.

4.2 Over-load Protection

When the output power just exceeds the 90W peak value, OLP triggers and the part enters hiccup mode as shown in Figure 16 and Figure 17.

Figure 16 shows the dynamic output transient from 60W to 90W with 100ms duration, separately, and that the device can handle this required nominal power.

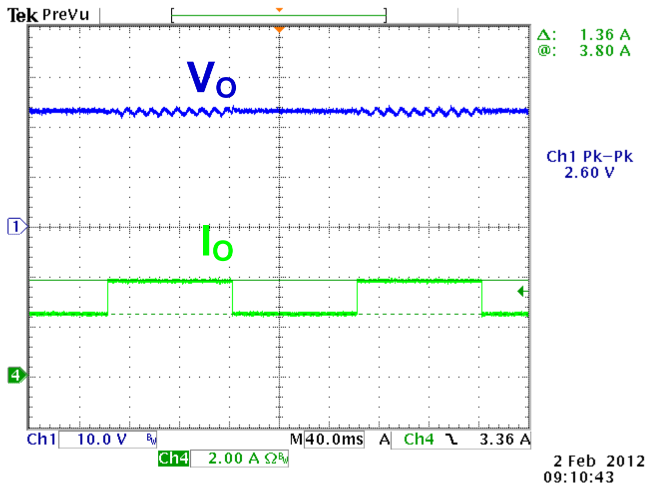

Figure 16: 60W to 90W Transient at Low Line Input (90V_{AC})

Figure 17 shows the output dynamic transient from 60W to 93W with 100ms duration, separately. It cannot sustain the 93W output for 100ms and the output voltage quickly drops to zero since OLP is triggered. Part enters hiccup mode at this time. This shows that even small margins need optimized transformer sizes for significant cost saving.

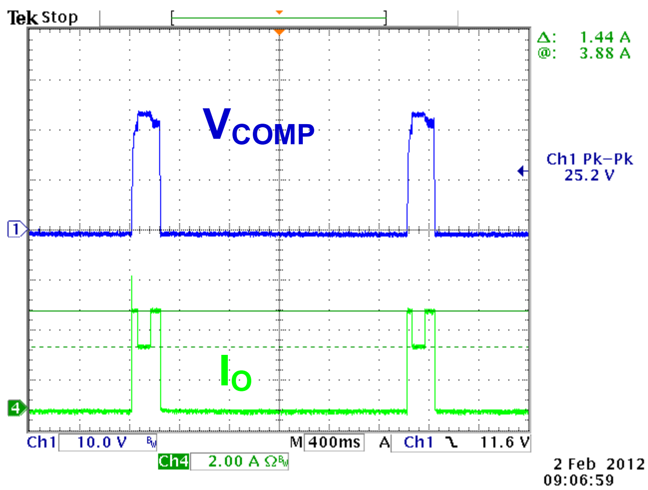

Figure 17: 60W to 93W Transient at Low Line Input (90V_{AC})

4.3 Load Regulation

Figure 18 shows the load regulation at various input voltages. To guarantee 90W peak power at low line ($90V_{AC}$), leave some power margin for high line inputs.

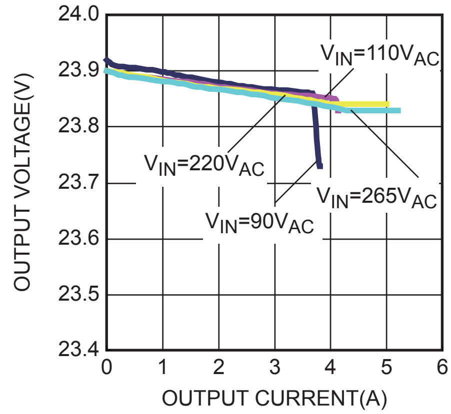

Figure 18: Load Regulation

4.4 Efficiency

Figure 19 shows the measured efficiency. Based on the efficiency curve, the efficiency exceeds than 85% with a load between 25% to 100%.

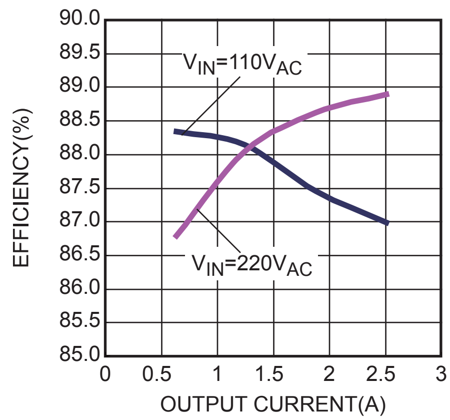

Figure 19: Efficiency vs. Load

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