PIN FUNCTIONS

SOIC8-7A Pin #	Name	Description
1	VCC	Supply. IC begins functioning when V_{CC} charges to V_{CCH} through an internal high-voltage current source. When V_{CC} falls below V_{CCL}, the internal high-voltage current source turns on to charge V_{CC}. Connect 0.1μF decoupling ceramic capacitor for most applications.
3	FB	Feedback. Provides the output reference voltage and detects falling voltage edges to determine the operation mode (CV mode and CC mode).
4	CP	Output Cable Compensation. Connect a 1μF ceramic capacitor as a low pass filter. The upper resistor of resistor divider connected to FB adjusts the compensation voltage.
2, 5, 6	GND	Ground.
8	Drain	Internal MOSFET Drain. Input for the high-voltage start-up current source.

FUNCTIONAL BLOCK DIAGRAM

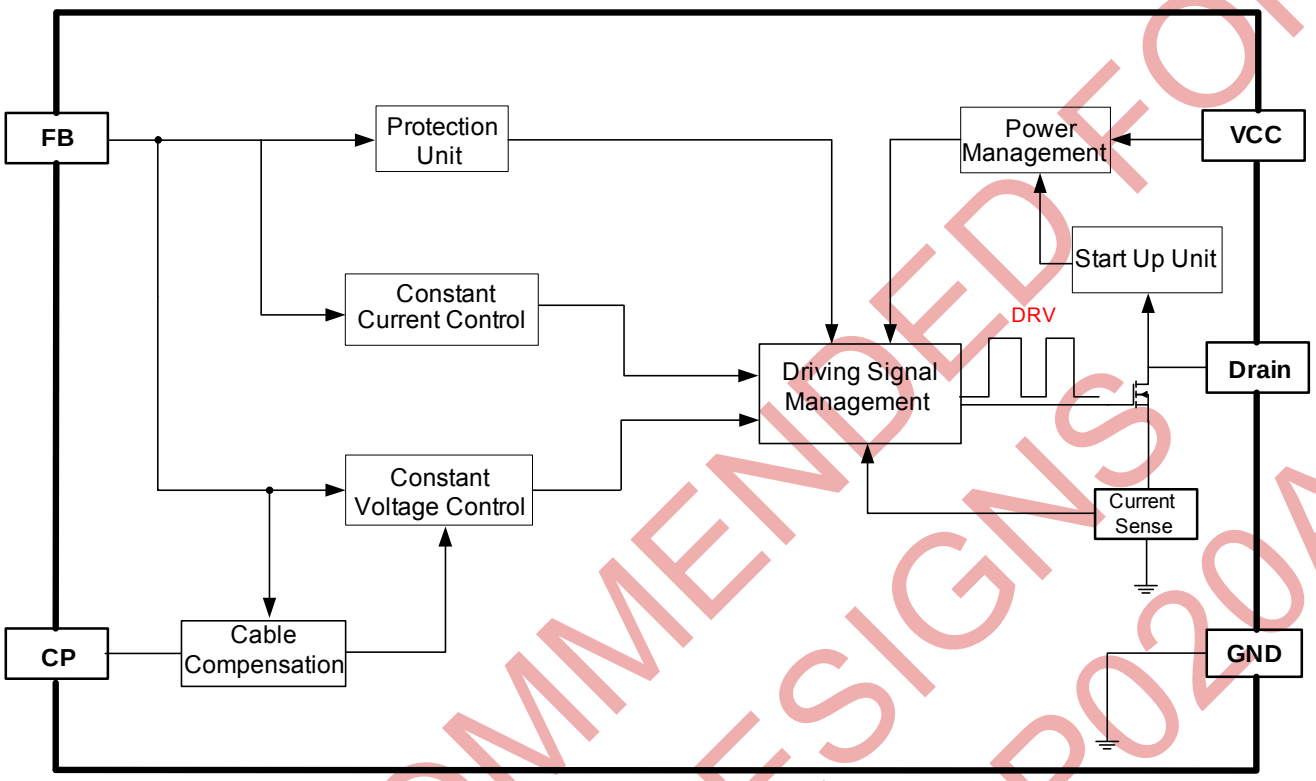


Figure 1: Functional Block Diagram

OPERATION

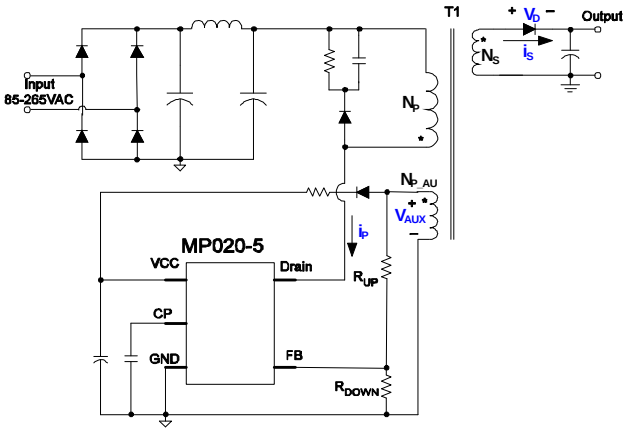


Figure 2: Simplified Flyback Converter

Startup

Initially, the IC is self-supplying through the internal high-voltage current source, which is drawn from the Drain pin. The internal high-voltage current source will turn off for better efficiency when V_{CC} reaches the V_{CC} ON threshold. Then the transformer's auxiliary winding takes over as the power source. When V_{CC} falls below the V_{CC} OFF threshold, the IC stops switching and the internal high-voltage current source turns on again. See Figure 3 for the start-up waveform.

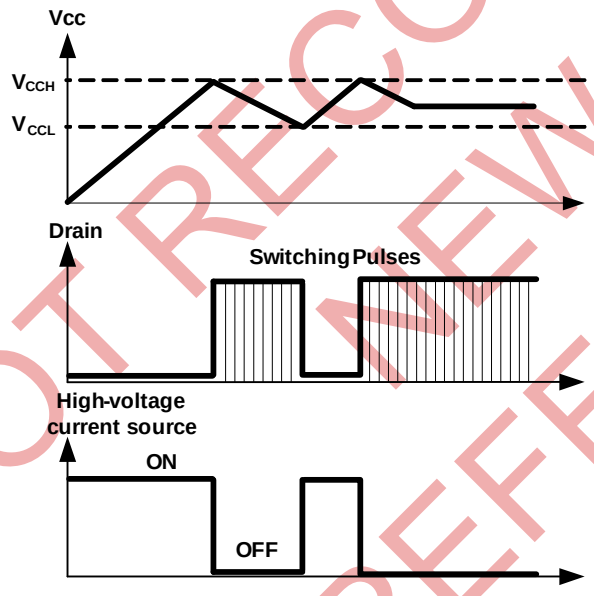


Figure 3: V_{CC} UVLO

Working Principle

After startup, the internal MOSFET turns on and the current sense resistor (R_{CS}) senses the primary current $i_P(t)$ internally. The current rises linearly at a rate of:

$$\frac{di_P(t)}{dt} = \frac{V_{IN}}{L_M}$$

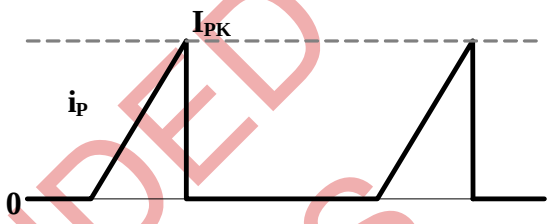


Figure 4: Primary Current Waveform

As illustrated in Figure 4, when $i_P(t)$ rises up to I_{PK}, the internal MOSFET turns off. Then, the energy stored in the inductor transfers to secondary-side through the transformer.

The inductor, L_M, stores energy with each cycle as a function of:

$$E = \frac{1}{2} L_M \times I_{PK}^2$$

So the power transferred from the input to the output is:

$$P = \frac{1}{2} L_M \times I_{PK}^2 \times f_S$$

Where f_S is the switching frequency. When I_{PK} is constant, the output power depends on f_S.

Constant-Voltage Operation

The MP020-5 detects the auxiliary winding voltage from the FB pin and operates in constant voltage (CV) mode to regulate the output voltage.

Assume the secondary winding is the master and the auxiliary winding is the slave. When the secondary-side diode turns on, the FB pin voltage is:

$$V_{FB} = \frac{N_{P\_AU}}{N_S} \times (V_O + V_D) \times \frac{R_{DOWN}}{R_{UP} + R_{DOWN}}$$

Where

- V_D is the secondary-side-diode forward-drop voltage,
- Vo is the output voltage,
- N_{P_AU} and N_S are the number of auxiliary winding and secondary side winding turns (respectively), and
- R_{UP} and R_{DOWN} are the resistor-divider for sampling.

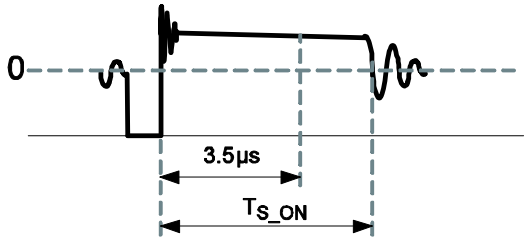


Figure 5: Auxiliary Voltage Waveform

The output voltage differs from the secondary voltage due to the current-dependant forward-diode voltage drop. If the secondary voltage is always detected at a fixed secondary current, the difference between the output voltage and the secondary voltage is a fixed V_D. The MP020-5 samples the auxiliary winding voltage 3.5µs after the primary switch turns off. The CV loop control function turns the secondary side diode off to regulate the output voltage.

Constant Current Operation

Figure 6 shows the constant-current operation.

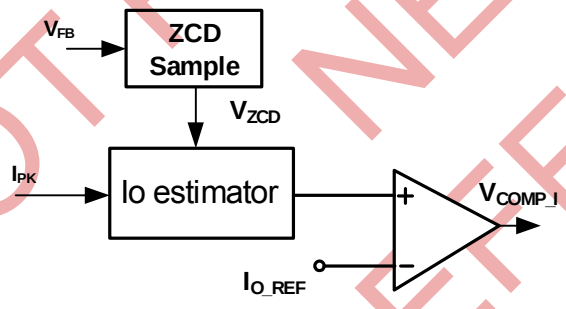


Figure 6: CC Control Loop

The flyback always works in DCM, and the ZCD sample block can detect the duty cycle of the secondary-side diode.

In constant current (CC) operation, the product of V_{ZCD} and I_{pk} approximately equals I_{O_REF}:

$$I_{O\_REF} = V_{ZCD} \times I_{PK}$$

So, the calculated output current from the I_O estimator block compares with reference value, I_{O_REF}, and the error signal, V_{COMP_I}, controls the turn on signal of the integral MOSFET. So I_O is then.

$$I_O = \frac{1}{2} \times \frac{N_P}{N_S} \times I_{O\_REF}$$

The MP020-5 maintains I_{O_REF} as 0.152A.

Leading-Edge Blanking

The parasitic capacitances induce a spike on the sense resistor when the power switch turns on. The MP020-5 includes a 300ns leading-edge blanking period to avoid falsely terminating the switching pulse. During this blanking period, the current sense comparator is disabled and the gate driver can not switch off. Figure 7 shows the leading-edge blanking.

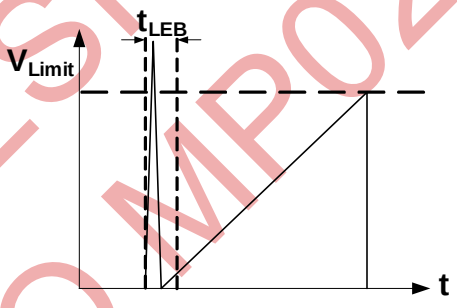


Figure 7: Leading-Edge Blanking

DCM Detection

The MP020-5 operates in discontinuous conduction mode (DCM) in both CV and CC modes. To avoid operating in continuous conduction mode (CCM), the MP020-5 detects the falling edge of the FB input voltage with each cycle. If the chip does not detect a 120mV falling edge, it will stop switching.

OVP & OCkP

The MP020-5 includes over-voltage protection (OVP) and open-circuit protection (OCkP). If the voltage at the FB pin exceeds 6.35V for 3.5μs, or the FB input's 0.15V falling edge cannot be monitored, the MP020-5 immediately shuts off the driving signals and enters hiccup mode. The MP020-5 resumes normal operation when the fault has been removed.

Thermal Shutdown (TSD)

When the temperature of the IC exceeds 150°C, over-temperature protection (OTP) triggers and the IC enters the auto recovery mode. When the temperature falls below 120°C, the IC will recover.

Output Cable Compensation

In order to compensate the secondary side cable voltage drop for a more precise output voltage, the MP020-5 has an internal output cable compensation circuit as shown in Figure 8. The internal ZCD sample can detect the duty of the secondary-side diode. A low-pass filter converts the duty signal to a DC voltage (V_{CP}) that changes as the load current varies.

V_{CP} can be converted to a current signal drawn from the FB pin. The voltage drop on R_{UP} helps the output cable compensation. When the system operates in maximum load, the CP pin voltage reaches a maximum of 2V.

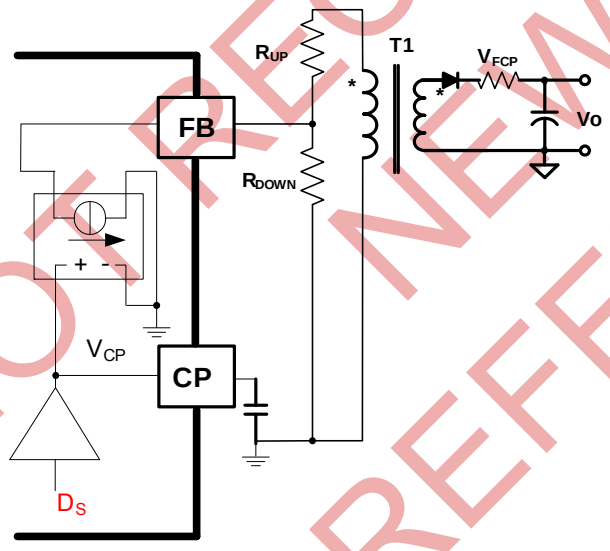


Figure 8: Output Cable Compensator

The equation below determines the compensation voltage:

$$V_{FCP} = \frac{5.6 \times D_S}{360 \times 10^3} \times 2 \times R_{UP} \times \frac{N_S}{N_{P\_AU}};$$

Where:

- V_{FCP} is the secondary-side compensation voltage drop,
- D_S is the secondary-diode duty cycle in CC mode (0.4 for the MP020-5),
- R_{UP} is the upper resistor of resistor divider,
- N_S is the number of turns for the secondary-side transformer windings, and
- N_{P_AU} is the number of transformer auxiliary winding turns.

APPLICATION INFORMATION

COMPONENT SELECTION

Input Filter

The input filter helps convert the AC input to a DC source through the rectifier. Figure 9 shows the input filter, and Figure 10 shows the typical DC bus voltage waveform.

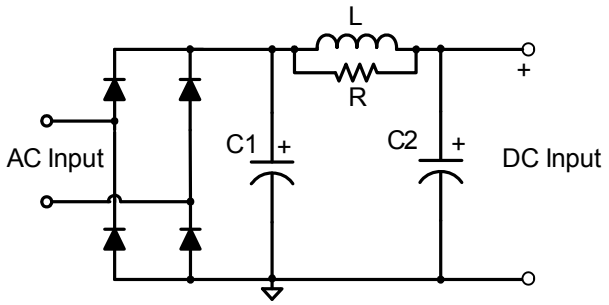


Figure 9: Input Filter

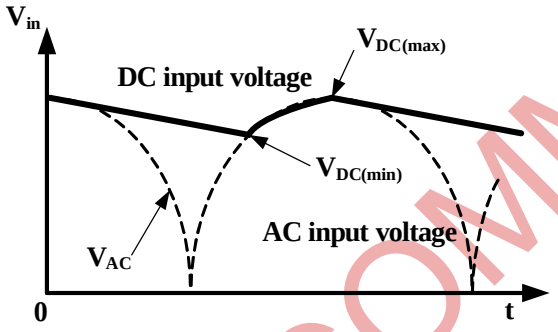


Figure 10: DC Input Voltage Waveform

Bulk capacitors (C1 and C2) filter the rectified AC input. The inductor (L) forms a π filter with C1 and C2 to restrain the differential-mode EMI noise. The resistor (R) in parallel with L restrains the mid-frequency-band EMI noise. Normally, the R is 1kΩ to 10kΩ.

C1 and C2 are usually set 2μF/W to 3μF/W for the universal input condition. For 230VAC single-range applications, halve the capacitor values. Avoid very low minimum DC voltages to ensure that the converter can supply the maximum power load, which can be expressed as:

$$V_{DC(min)} \geq \frac{N_P}{N_S} \cdot (V_O + V_D) \cdot \frac{D_S}{1 - D_S}$$

If $V_{DC(min)}$ can not satisfy this expression, increase the value of the input capacitors to increase the $V_{DC(min)}$.

Output Capacitor

Use low ESR or very low ESR output capacitors to meet the output voltage ripple requirement without using an LC post filter. In addition, using low ESR capacitors improves output voltage regulation and feedback voltage sampling at high temperatures or low temperatures. Use an output capacitor with an ESR lower than 100mΩ for better efficiency over non-low ESR output capacitors.

Output Diode

Use a Schottky diode because of its fast switching speed and low forward-voltage drop for better high or low temperature CV regulation and efficiency.

If the lower average efficiency (3% to 4%) is acceptable, replace the output diode could with a fast or ultra-fast diode to reduce costs. Be sure to readjust the resistor divider values to for the correct output voltage because of the forward voltage drop is higher than the Schottky diode's.

Leakage Inductance

The transformer's leakage inductance will decrease the system efficiency and affect the output current or voltage constant precision. Optimize the transformer structure to minimize the leakage inductance. Aim for a leakage inductance less than 5% of the primary inductance.

RCD Snubber

The transfomer's leakage inductance causes the MOSFET drain voltage to spike and the excessive ringing on the drain voltage waveform, which affects the output voltage sampling 3.5μs after the MOSFET turns off.

The RCD snubber circuit can limit the Drain voltage spike. Figure 11 shows the RCD snubber circuit.

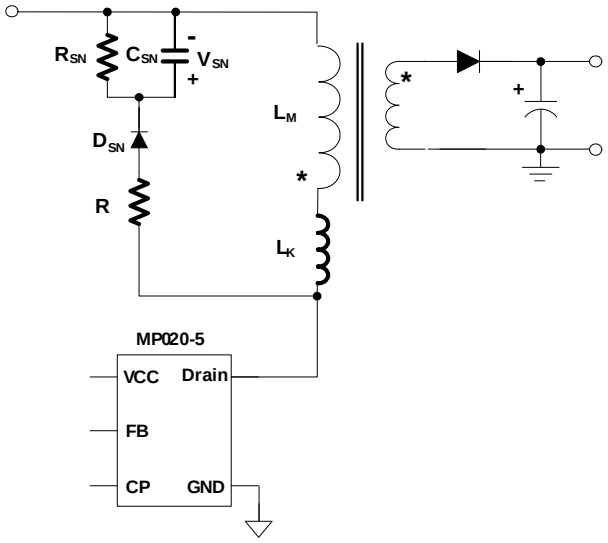


Figure 11: RCD Snubber

Select R_{SN} and C_{SN} to meet the voltage spike requirements and improve system operation.

The power dissipated in the snubber circuit is approximately.

$$P_{SN} = \frac{1}{2} \cdot L_K \cdot I_{PK}^2 \cdot \frac{V_{SN}}{V_{SN} - N_{PS} \times V_O} \times f_S$$

Where:

- L_K is the leakage inductance,
- V_{SN} is the clamp voltage, and
- N_{PS} is the turn ratio of primary and secondary side.

Since R_{SN} consumes the majority of the power, R_{SN} is approximately,

$$R_{SN} = \frac{V_{SN}^2}{P_{SN}}$$

The maximum ripple of the snubber capacitor voltage is then:

$$\Delta V_{SN} = \frac{V_{SN}}{C_{SN} \cdot R_{SN} \cdot f_S}$$

Generally, 15% ripple is reasonable, So the previous equation can estimate C_{SN}.

Normally, select a time constant ($\tau = R_{SN} \times C_{SN}$) less than 0.1ms for better CV sampling. Therefore, adjust the resistor based on the power loss and the acceptable clamp voltage in practical applications.

The damping resistor in series with the RCD has a relatively large value to prevent any excessive voltage ringing that can affect the CV sampling and increase the output ripple. Use a damping resistor value in the range of 200Ω to 500Ω to restrain the drain-voltage ringing.

Divided Resistor

For better application performance, the select the resistor divider values from 10kΩ to 100kΩ to limit noise from adjacent components on the FB pin. If necessary, use a resistor between 1kΩ and 2kΩ connected between the FB pin and resistor divider limit substrate-injection-current effects, as shown in Figure 12.

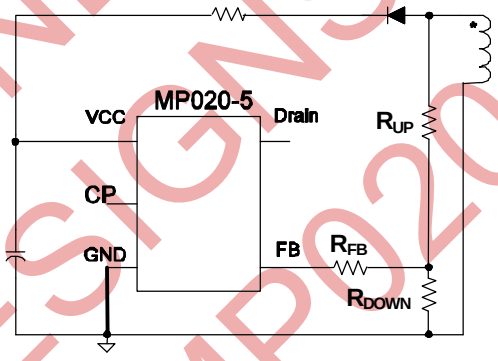


Figure 12: Feedback Resistor Divider Circuit

For more accurate CV regulation, the accuracy of these feedback resistors should be at least 1%.

Dummy Load

When system operates without any load and no dummy load, the output voltage will rise above normal operation because of the minimum switching frequency limitation. Use a dummy load for good load regulation. A large dummy load will deteriorate efficiency and no-load consumption, so the dummy load is tradeoff between efficiency and load regulation. For most applications, use a dummy load of around 10mW as it also satisfies the 30mW requirement.

Maximum Switching Frequency

Use a secondary-side diode conduction time that exceeds 5.4μs, as per the following equation.

$$T_{S\_ON} = I_{PK} \cdot \frac{N_S \cdot L_M}{N_P \cdot (V_O + V_D)} > 5.4\mu s$$

For high- or low-temperature applications, select a maximum switching frequency below 75kHz.

PCB Layout Guide

PCB layout is very important to achieve reliable operation, good EMI, and good thermal performance. The following describe some layout recommendations.

1. Minimize the loop area formed by the input capacitor, the MP020-5 drain-source, and the primary winding to reduce EMI noise.

2. The copper area connected to GND pins is the heat conduction path for the MP020-5. Provide at least 1 in^2 of top-side copper for adequate heat-sinking.

3. Minimize the clamp circuit loop to reduce EMI.

4. Minimize the secondary loop area of the output diode and output filter to reduce EMI noise. In addition, sufficient copper area should be provided at the anode and cathode terminal of the output diode to act as a heat sink.

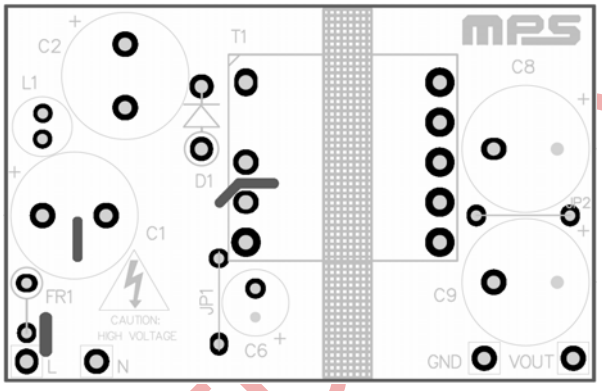
5. Place the AC input away from the switching nodes to minimize the noise coupling that may bypass the input filter.

6. Place the bypass capacitor as close as possible to the IC and source.

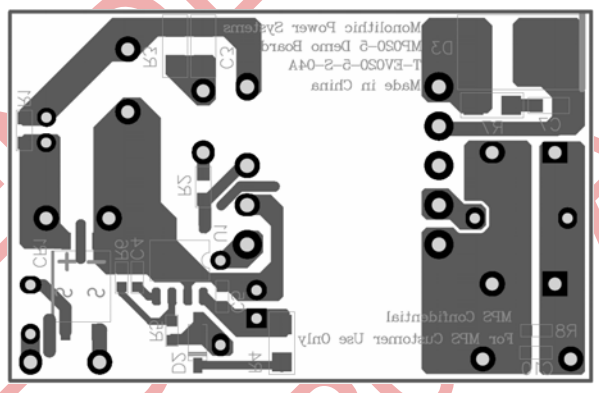
7. Place the feedback resistors next to the FB pin and minimize the feedback sampling loop to minimize noise coupling.

8. Use a single point connection at the negative terminal of the input filter capacitor for the MP020-5 source pin and bias winding return.

Figure 13 shows a sample layout.



Top Layer



Bottom Layer

Figure 13: PCB Layout

Design Example

Below is a design example following the application guidelines based on these specifications:

Table 1: Design Example

V_{IN}	85Vac~265Vac
V_{OUT}	5V
I_{OUT}	1A
f_S	60kHz

Figure 14 shows the detailed application schematic This circuit was used for the typical performance and circuit waveforms. For more device applications, please refer to the related evaluation board datasheets.

The transformer structure used in figure 14 could be benefit to pass the 3 wire Conducted

EMI (Output GND connect to earth) without Y cap. The Y cap will bring about the leakage current which is prohibited in some cell phone charger application. Figure 15 could illustrate how the Common Noise of the secondary side diode be restrained. The secondary side winding split to two separate windings N_{SEC1} and N_{SEC2} which have same turns and approximate parasitic capacitor C_{SP1},and C_{SP2} but their 'hot spot' is opposite as the Point 9 and Point 10 in Figure 15, so the common mode noise current produced at secondary side windings can be counteracted each other.

The transformer structure could be simple if the application does not need to pass the 3 wire Conducted EMI or could use the Y cap. Figure 16 shows the schematic with the simple transformer structure.

TYPICAL APPLICATION CIRCUITS

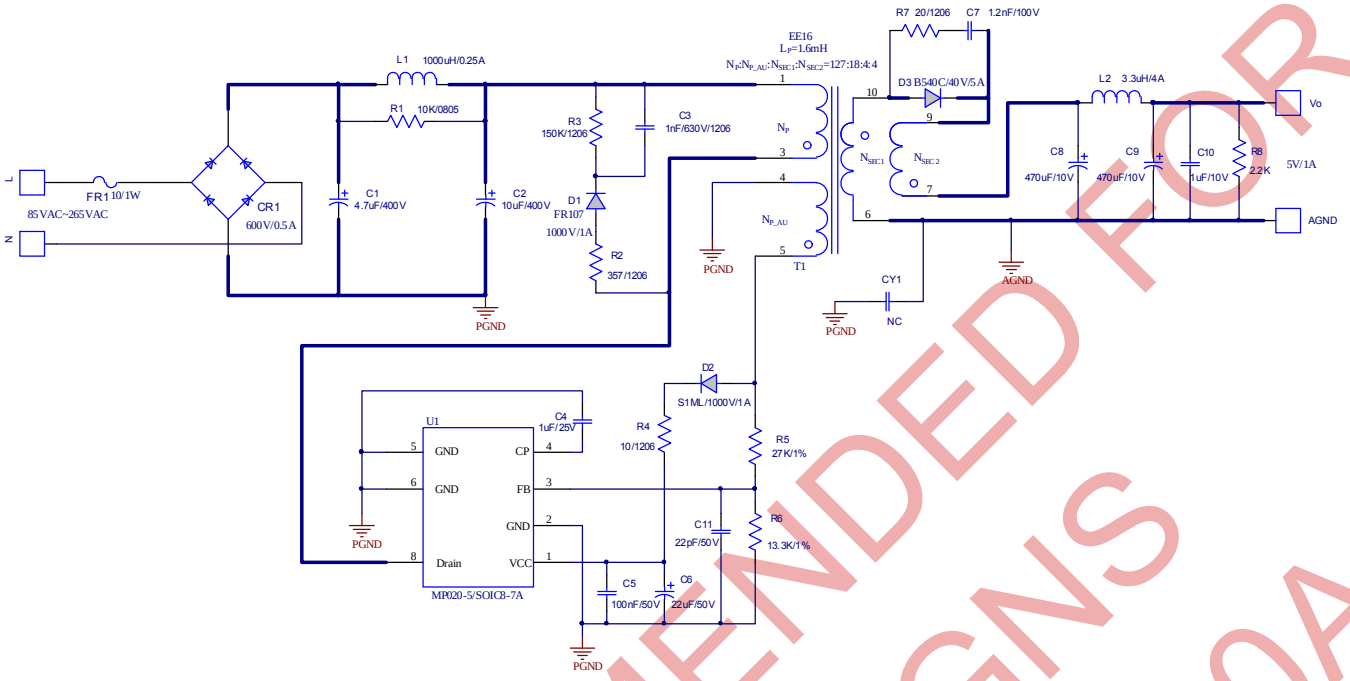


Figure 14: Typical Application, 5V/1A with Complicated Transformer Structure

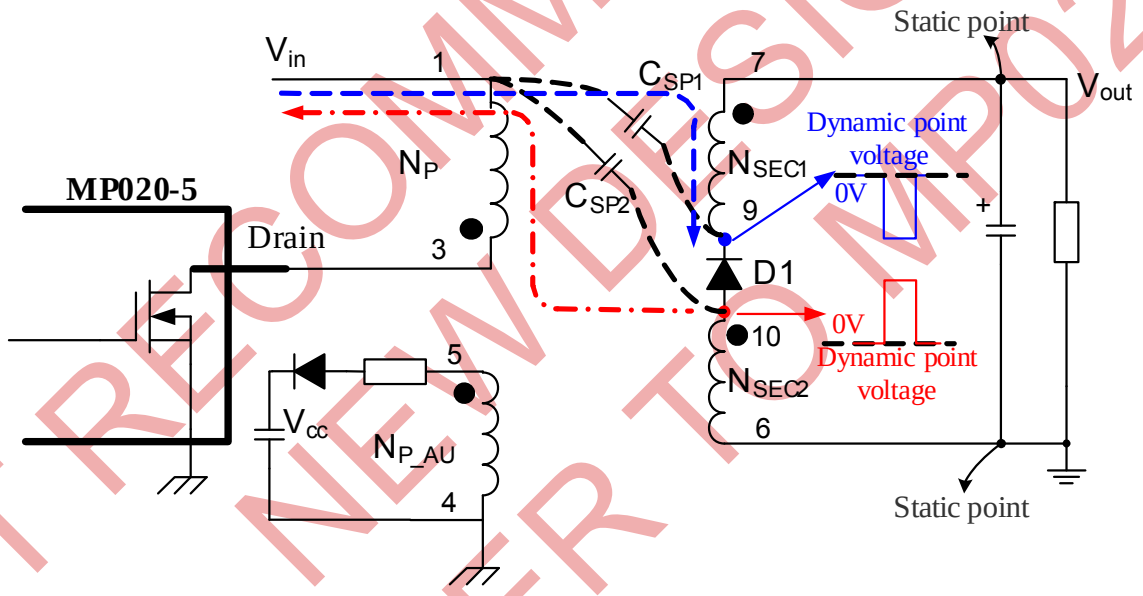


Figure 15: Secondary Side Windings Structure to Restrain the Common Mode Noise

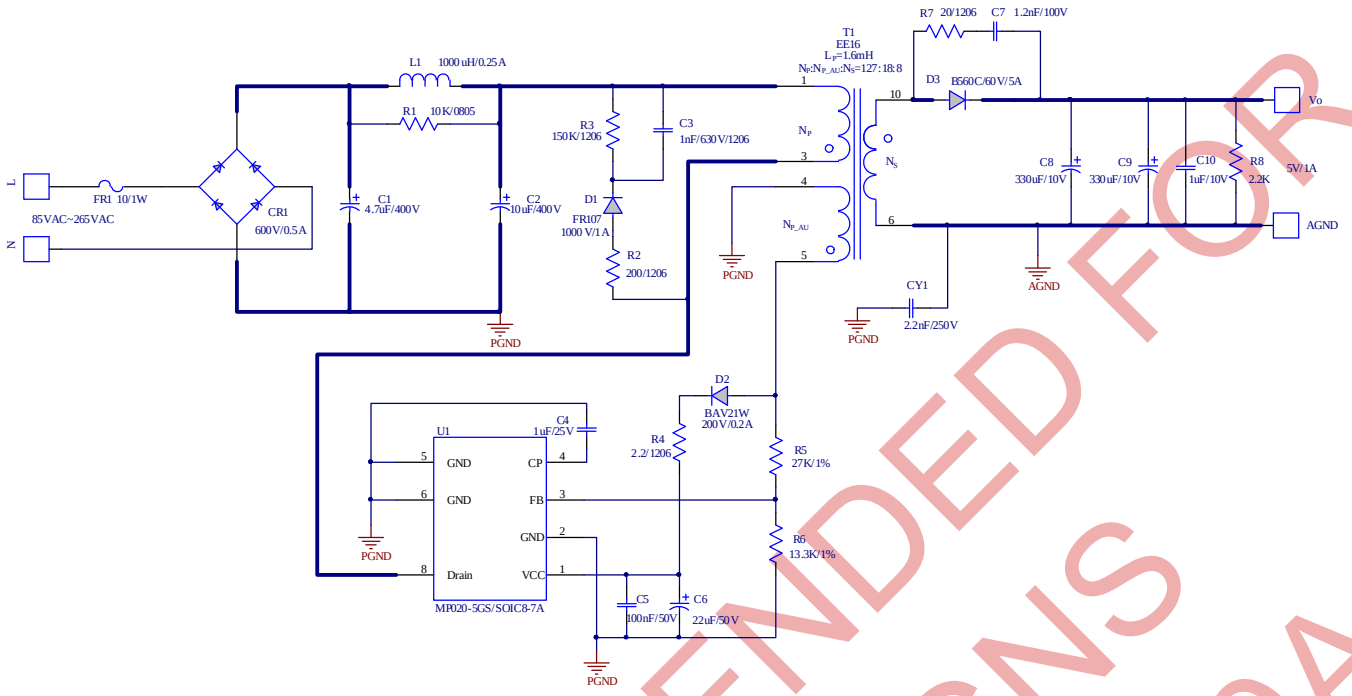
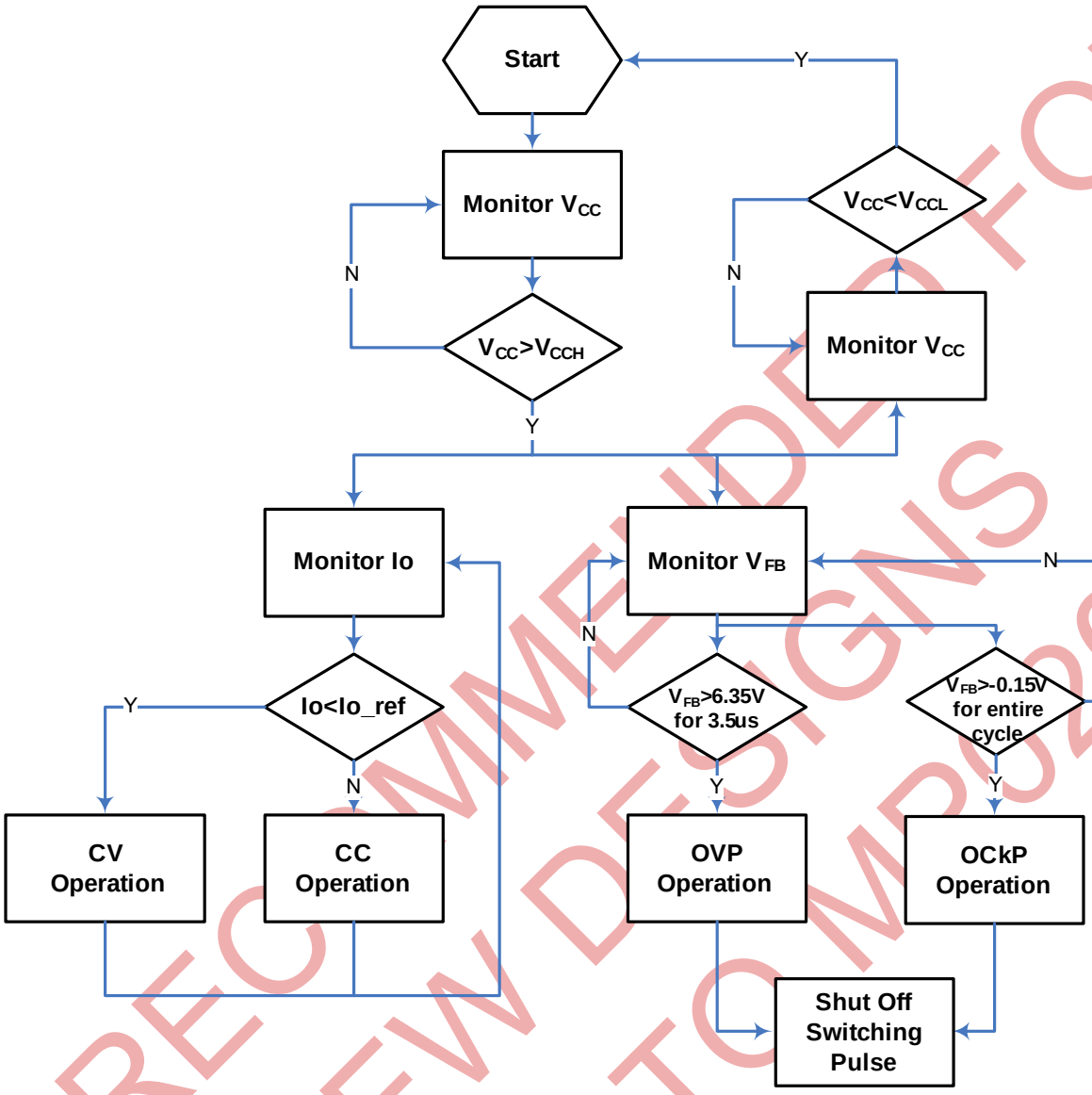


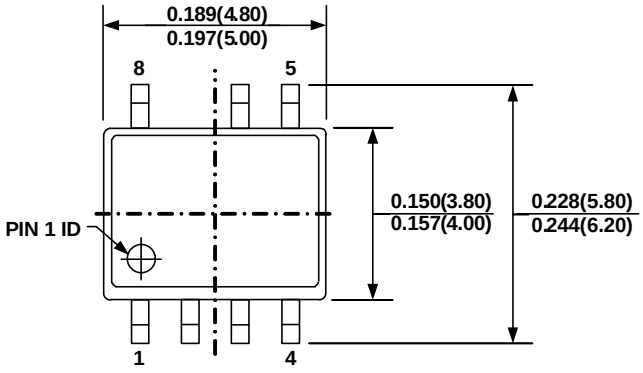
Figure 16: Typical Application, 5V/1A with Simple Transformer Structure

FLOW CHART

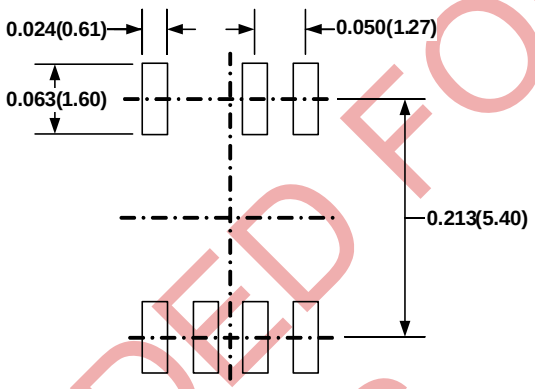


PACKAGE INFORMATION

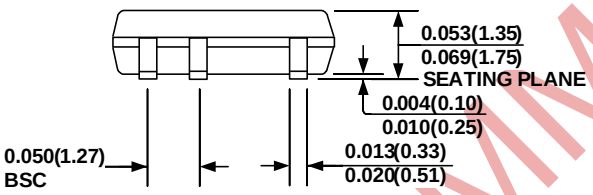
SOIC8-7A



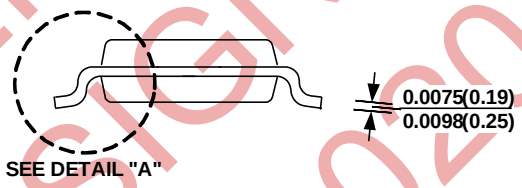
TOP VIEW



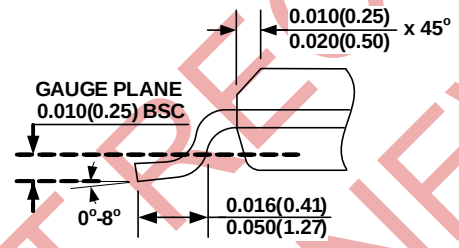
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) JEDEC REFERENCE IS MS-012.
6) DRAWING IS NOT TO SCALE